2.5/3V 4M/2M/1M -BIT SERIAL FLASH MEMORY WITH DUAL/QUAD SPI, QPI & DTR

Industrial Plus Grade

Publication Release Date: February 18, 2025
-Revision D

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1. GENERAL DESCRIPTIONS

The W25Q40/20/10RL (4/2/1M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.3 V to 3.6V power supply with current consumption as low as 0.1µA for power-down.

The W25Q40/20/10RL arrays are organized into 2048/1024/512 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. The W25Q40/20/10RL have 128 /64/32 erasable sectors, 16/8/4 erasable 32KB blocks and 8/4 erasable 64KB blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 2.)

The W25Q40/20/10RL supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2(/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 532MHz (133MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O commands. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Read Command Bypass Mode allows for efficient memory access with as few as 8-clocks of command-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  – W25Q40RL: 4M-bit /512K-byte (524,288)
  W20Q20RL: 2M-bit /256K-byte (262,144)
  W20Q10RL: 1M-bit /128K-byte (131,072)
  – Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  – Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  – Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  – Software & Hardware Reset(1)
- **Highest Performance Serial Flash**
  – 133MHz Single, Dual/Quad SPI clocks
  – 266/532MHz equivalent Dual/Quad SPI
  – 66MB/S continuous data transfer rate
  – Min. 100K Program-Erase cycles
  – More than 20-year data retention
- **Efficient "Continuous Read"**
  – Continuous Read with 8/16/32/64-Byte Wrap
  – As few as 8 clocks to address memory
  – Allows true XIP (execute in place) operation
  – Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  –Single 2.3 to 3.6V supply
  – -40°C to +105°C operating range
  – <0.1µA Power-down (typ.)
- **Flexible Architecture with 4KB sectors**
  – Uniform Sector/Block Erase (4K/32K/64K-Byte)
  – Program 1 to 256 byte per programmable page
  – Erase/Program Suspend & Resume
- **Advanced Security Features**
  – Software and Hardware Write-Protect
  – Power Supply Lock-Down and
  – Special OTP protection(2)
  – Top/Bottom, Complement array protection
  – 64-Bit Unique ID for each device
  – Discoverable Parameters (SFDP) Register
  – 3X256-Bytes Security Registers with OTP locks
  – Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging:**
  – 8-pin SOIC 150-mil
  – 8-pin SOIC 208-mil
  – 8-pad XSON 2X3mm(2)
  – Contact Winbond for KGD and other options

Note: 1. Hardware /RESET pin is only available on SOIC-16 & TFBGA packages
2. Please contact Winbond for details.

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOIC 150/208-mil

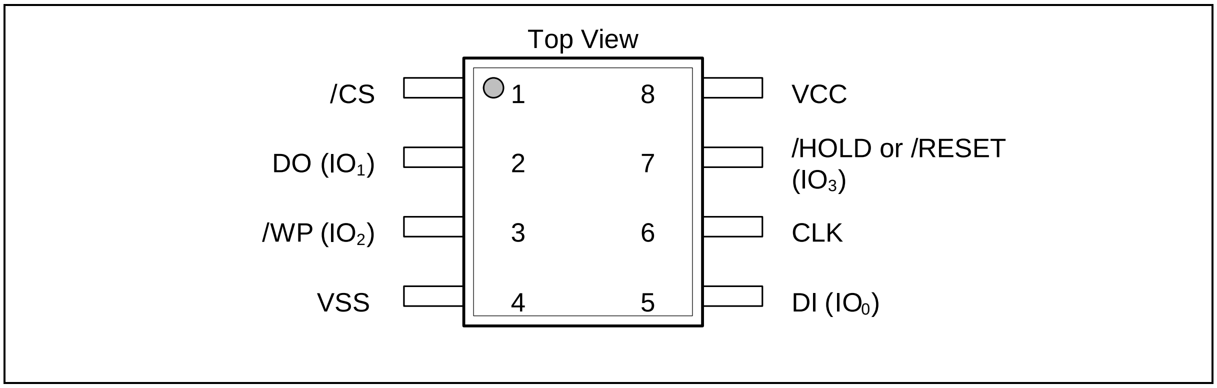

Figure 1a. Pin Assignments, 8-pin SOIC 150/208-MIL (Package Code SN, SS)

3.2 Pad Configuration XSON 2x3-mm

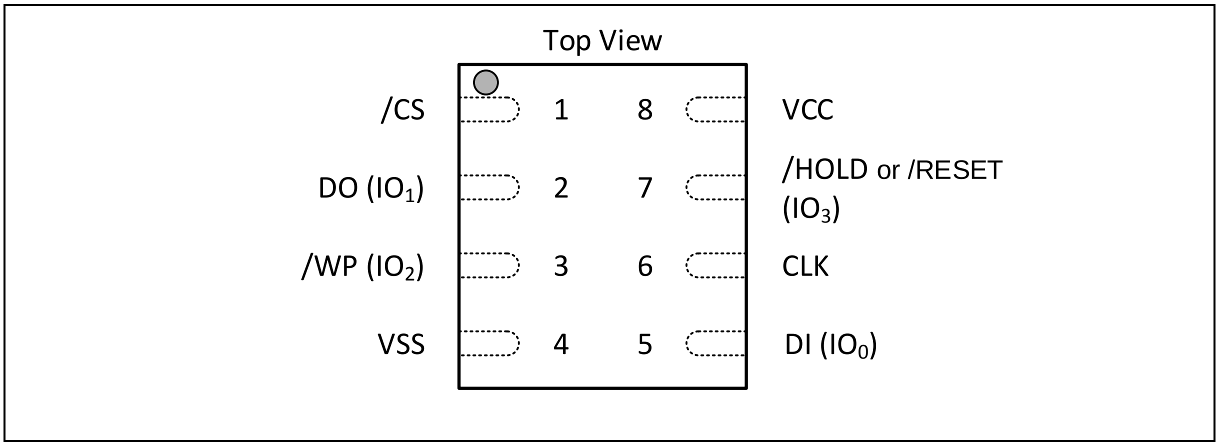

Figure 1b. Pad Assignments, 8-pad XSON 2X3-mm (Package Code XH)

3.3 Pin Description SOIC 150/208-mil, XSON 2x3-mm

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI commands
2. IO0 – IO3 are used for Quad SPI commands, /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and commands can be written to and data read from the device. After power-up, /CS must transition from high to low before a new command will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q40/20/10RL supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI commands use the unidirectional DI (input) pin to serially write commands, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI commands use the bidirectional IO pins to serially write commands, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, /HOLD pin becomes IO3.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

4.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 1a-e for the pin configuration of Quad I/O operation.

4.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin configuration. On the 16-pin SOIC package, a dedicated /RESET pin is provided and it is independent of QE bit setting.

5. BLOCK DIAGRAM

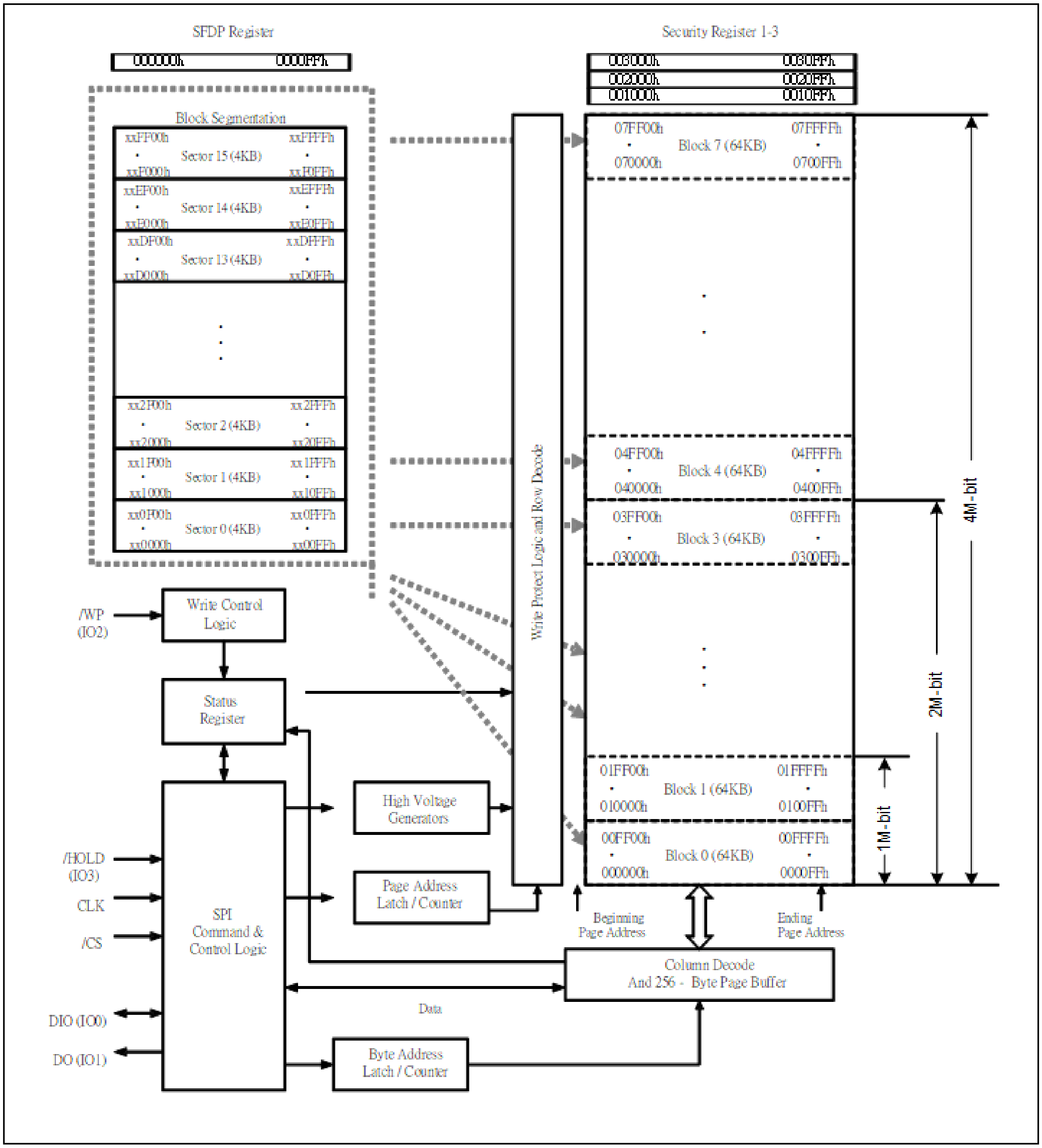

Figure 2. W25Q40/20/10RL Serial Flash Memory Block Diagram

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6. FUNCTIONAL DESCRIPTIONS

6.1 SPI / QPI Operations

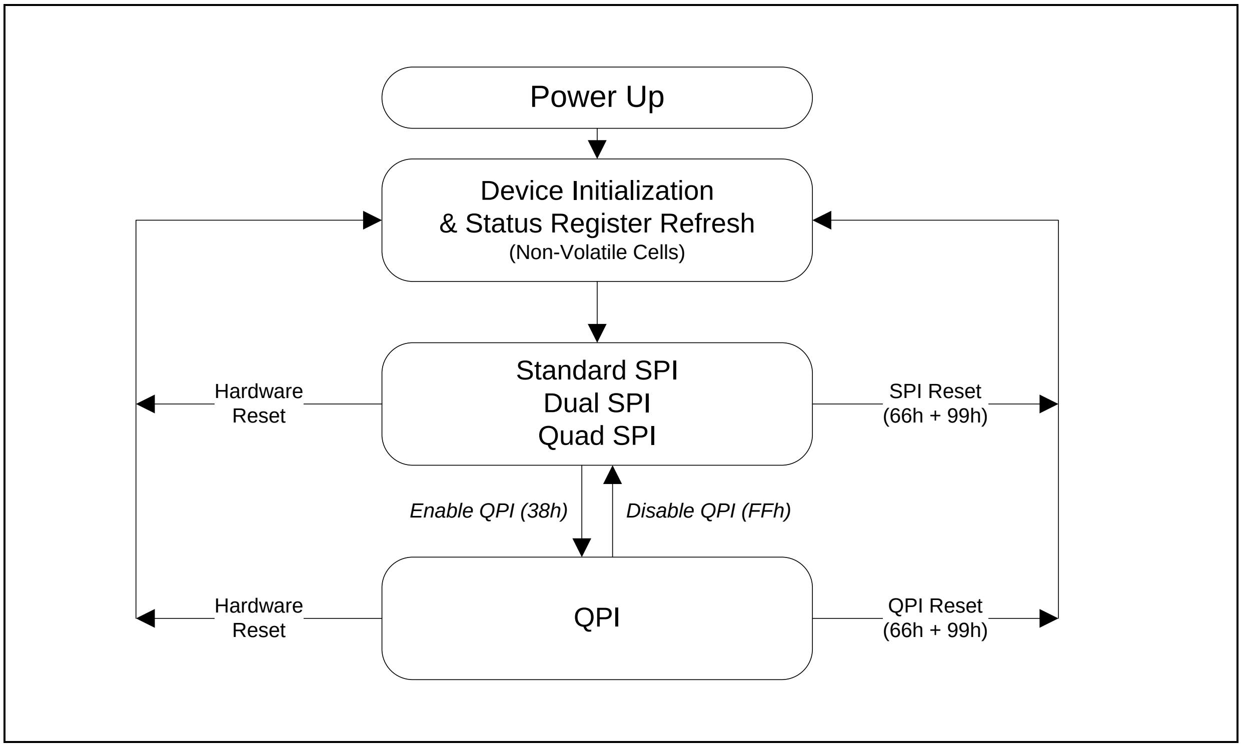


Figure 3. W25Q40/20/10RL Serial Flash Memory Operation Diagram

6.1.1 Standard SPI Commands

The W25Q40/20/10RL is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI commands use the DI input pin to serially write commands, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Commands

The W25Q40/20/10RL supports Dual SPI operation when using commands such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These commands allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read commands are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI commands, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Commands

The W25Q40/20/10RL supports Quad SPI operation when using commands such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh). These commands allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read commands offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI commands the DI and DO pins become bidirectional IO0 and IO1, and the /HOLD pin becomes IO3 respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.1.4 QPI Commands

The W25Q40/20/10RL supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” command. The typical SPI protocol requires that the byte-long command code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the command code, thus only two serial clocks are required. This can significantly reduce the SPI command overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” commands are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” command, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI commands, the DI and DO pins become bidirectional IO0 and IO1, and the /HOLD pin becomes IO3 respectively. See Figure 3 for the device operation modes.

6.1.5 SPI / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, W25Q40RV introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

6.1.6 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25Q40/20/10RL operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the command and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD, when QE=1, the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.1.7 Software Reset & Hardware /RESET pin

The W25Q40/20/10RL can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS (t_{RST}) to reset. No command will be accepted during the reset period.

For the WSON-8 and TFBGA package types, W25Q40/20/10RL can also be configured to utilize a hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any command input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pins.

For the SOIC-16 package, W25Q40/20/10RL provides a dedicated /RESET pin in addition to the /HOLD (IO_3) pin as illustrated in Figure 1b. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated /RESET pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the SOIC-16 package. If the reset function is not needed, this pin can be left floating in the system.

6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q40/20/10RL provides several means to protect the data from inadvertent writes.

6.2.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable commands and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Write Protection using Power-down command
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special flow. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q40/20/10RL will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 58). While reset, all operations are disabled and no commands are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related commands are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register commands. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register command and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down command offers an extra level of write protection as all commands are ignored except for the Release Power-down command.

7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q40/20/10RL. The Read Status Register-1/2/3 commands can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register command can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, output driver strength and power-up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable command, and during Standard/Dual SPI operations, the /WP pin.

7.1 Status Registers

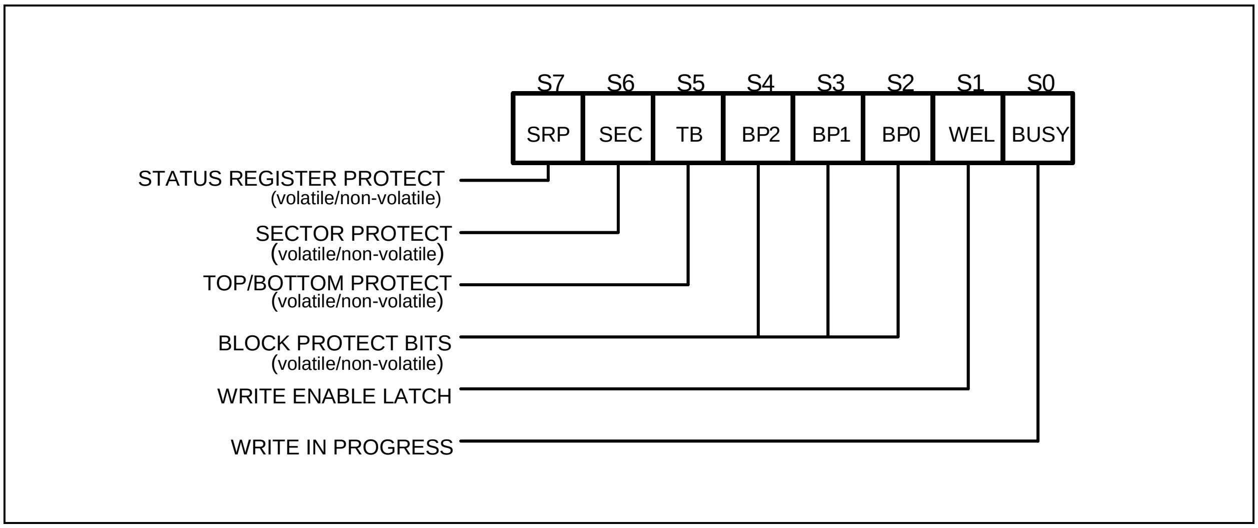


Figure 4a. Status Register-1

7.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register command. During this time the device will ignore further commands except for the Read Status Register and Erase/Program Suspend command (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register command has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further commands.

7.1.2 Write Enable Latch (WEL) – *Status Only*

The Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following Instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Command (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase commands (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Command depending on the state of the SRP, SRL and WEL bits.

7.1.5 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0

7.1.7 Status Register Protect (SRP, SRL)

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bit controls the method of write protection: software protection or hardware protection. The Status Register Lock bits (SRL) are non-volatile/volatile read/write bits in the status register (S8). The SRL bit controls the method of write protection: temporary lock-down or permanently one time program.

SRL	SRP	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable command, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable command, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	X	X	One Time Program(2)	Status Register is permanently protected and cannot be written to. (**enabled by adding prefix command AAh, 55h)**

Note:

1. When SRL =1, a power-down, power-up cycle will change the SRL =0 state.
2. Please contact Winbond for details regarding the special command sequence.

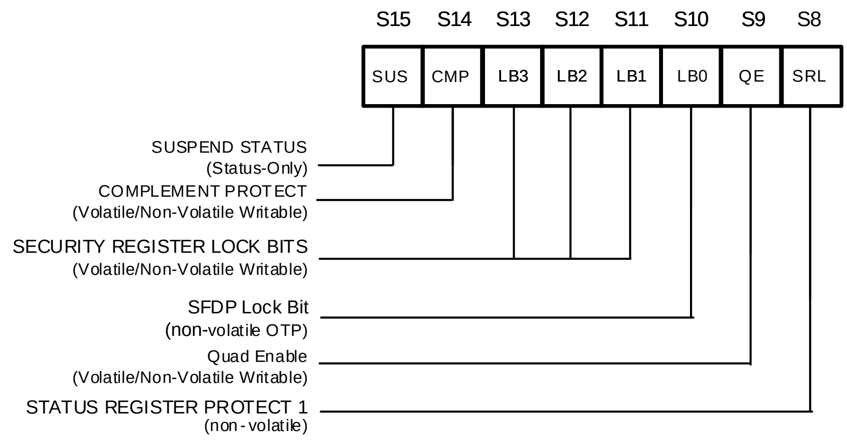


Figure 4b. Status Register-2

7.1.9 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) Instruction. The SUS status bit is cleared to 0 by the Erase/Program Resume (7Ah) Instruction as well as a power-down, power-up cycle.

7.1.10 Security Register Lock Bits (LB3, LB2, LB1, LB0) –*Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register Instruction. LB3-1 are One Time Programmable (OTP). Once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

The default state of LB0 is 1, SFDP Security Register is locked.

7.1.11 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options JM), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option "JQ"), the Quad IO2 and IO3 pins are enabled, and /HOLD function is disabled.

The QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the Instruction will be ignored. When the device is in QPI mode, the QE bit will remain a 1. A "Write Status Register" Instruction in QPI mode cannot change the QE bit from a "1" to a "0

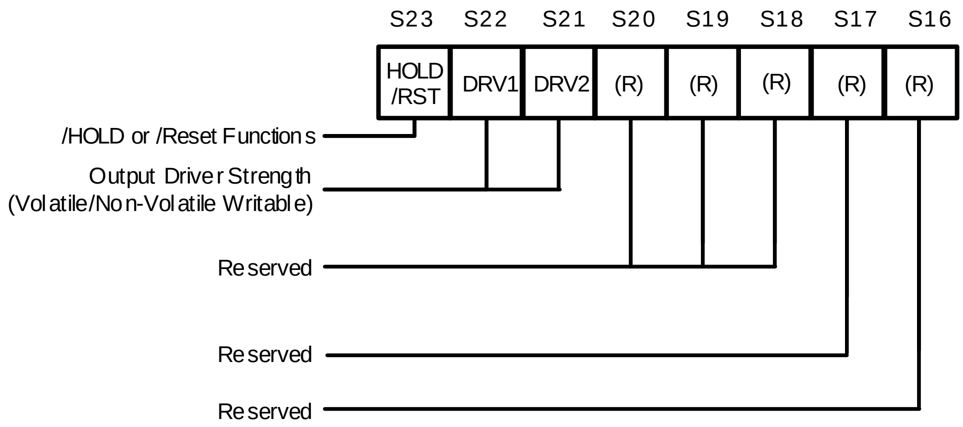


Figure 4c. Status Register-3

7.1.12 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Resistor
0, 0	25-ohm
0, 1	33-ohm
1, 0	50-ohm(default)
1, 1	100-ohm

7.1.13 /HOLD or /RESET Pin Function (HOLD/RST) – *Volatile/Non-Volatile Writable*

The HOLD/RST bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

7.1.14 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of these bits. During a “Write Status Register” command, the Reserved Bits can be written as “0”, but there will not be any effect.

7.1.15 W25Q40RL Status Register Memory Protection (CMP = 0)

STATUS REGISTER[1]					W25Q40RL (4M-BIT) MEMORY PROTECTION			
SEC	**TB**	**BP2**	**BP1**	**BP0**	**BLOCK(S)**	**ADDRESSES**	**DENSITY**	**PORTION**
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000h – 07FFFFh	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000h – 07FFFFh	128KB	Upper 1/4
0	0	0	1	1	4 thru 7	040000h – 07FFFFh	256KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/8
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/4
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/2
0	**X**	**1**	**0**	**0**	**0 thru 7**	**000000h – 07FFFFh**	**512KB**	**ALL**
0	**X**	**1**	**0**	**1**	**0 thru 7**	**000000h – 07FFFFh**	**512KB**	**ALL**
0	**X**	**1**	**1**	**X**	**0 thru 7**	**000000h – 07FFFFh**	**512KB**	**ALL**
1	0	0	0	1	7	07F000h – 07FFFFh	4KB	Top Block
1	0	0	1	0	7	07E000h – 07FFFFh	8KB	Top Block
1	0	0	1	1	7	07C000h – 07FFFFh	16KB	Top Block
1	0	1	0	**0**	7	078000h – 07FFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	0	0	000000h – 007FFFh	32KB	Bottom Block
1	X	1	1	1	0 thru 7	000000h – 07FFFFh	512KB	ALL

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program Instruction specifies a memory region that contains a protected data portion, this Instruction will be ignored.

7.1.16 W25Q40RL Status Register Memory Protection (CMP = 1)

STATUS REGISTER(1)					W25Q40RL (4M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 7	000000h – 07FFFFh	512KB	ALL
0	0	0	0	1	0 thru 6	000000h – 06FFFFh	448KB	Lower 7/8
0	0	0	1	0	0 thru 5	000000h – 05FFFFh	384KB	Lower 3/4
0	0	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/2
0	1	0	0	1	1 thru 7	010000h – 07FFFFh	448KB	Upper 7/8
0	1	0	1	0	2 thru 7	020000h – 07FFFFh	384KB	Upper 3/4
0	1	0	1	1	4 thru 7	040000h – 07FFFFh	256KB	Upper 1/2
0	**X**	**1**	**0**	**0**	NONE	NONE	NONE	NONE
0	**X**	**1**	**0**	**1**	NONE	NONE	NONE	NONE
0	**X**	**1**	**1**	**X**	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 7	000000h – 07EFFFh	508KB	Lower 127/128
1	0	0	1	0	0 thru 7	000000h – 07DFFFh	504KB	Lower 63/64
1	0	0	1	1	0 thru 7	000000h – 07BFFFh	496KB	Lower 31/32
1	0	1	0	**0**	0 thru 7	000000h – 077FFFh	480KB	Lower 15/16
1	1	0	0	1	0 thru 7	001000h – 07FFFFh	508KB	Upper 127/128
1	1	0	1	0	0 thru 7	002000h – 07FFFFh	504KB	Upper 63/64
1	1	0	1	1	0 thru 7	004000h – 07FFFFh	496KB	Upper 31/32
1	1	1	0	0	0 thru 7	008000h – 07FFFFh	480KB	Upper 15/16
1	X	1	1	1	NONE	NONE	NONE	NONE

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program Instruction specifies a memory region that contains a protected data portion, this Instruction will be ignored.

7.1.17 W25Q20RL Status Register Memory Protection (CMP = 0)

STATUS REGISTER[(1)]					W25Q20RL (2M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	3	030000h – 03FFFFh	64KB	Upper 1/4
0	0	0	1	0	2 and 3	020000h – 03FFFFh	128KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/4
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/2
0	X	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	ALL
0	X	1	X	X	0 thru 3	000000h – 03FFFFh	256KB	ALL
1	0	0	0	1	3	03F000h – 03FFFFh	4KB	Upper 1/64
1	0	0	1	0	3	03E000h – 03FFFFh	8KB	Upper 1/32
1	0	0	1	1	3	03C000h – 03FFFFh	16KB	Upper 1/16
1	0	1	0	0	3	038000h – 03FFFFh	32KB	Upper 1/8
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/64
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/32
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/16
1	1	1	0	0	0	000000h – 007FFFh	32KB	Lower 1/8
1	X	1	1	1	0 thru 3	000000h – 03FFFFh	256KB	ALL

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program Instruction specifies a memory region that contains a protected data portion, this Instruction will be ignored.

7.1.18 W25Q20RL Status Register Memory Protection (CMP = 1)

STATUS REGISTER[(1)]					W25Q20RL (2M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 3	000000h – 03FFFFh	256KB	ALL
0	0	0	0	1	0 thru 2	000000h – 02FFFFh	192KB	Lower 3/4
0	0	0	1	0	0 thru 1	000000h – 01FFFFh	128KB	Lower 1/2
0	1	0	0	1	1 thru 3	010000h – 03FFFFh	192KB	Upper 3/4
0	1	0	1	0	2 thru 3	020000h – 03FFFFh	128KB	Upper 1/2
0	X	0	1	1	NONE	NONE	NONE	NONE
0	X	1	X	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 3	000000h – 03EFFFh	252KB	Lower 63/64
1	0	0	1	0	0 thru 3	000000h – 03DFFFh	248KB	Lower 31/32
1	0	0	1	1	0 thru 3	000000h – 03BFFFh	240KB	Lower 15/16
1	0	1	0	0	0 thru 3	000000h – 037FFFh	224KB	Lower 7/8
1	1	0	0	1	0 thru 3	001000h – 03FFFFh	252KB	Upper 63/64
1	1	0	1	0	0 thru 3	002000h – 03FFFFh	248KB	Upper 31/32
1	1	0	1	1	0 thru 3	004000h – 03FFFFh	240KB	Upper 15/16
1	1	1	0	0	0 thru 3	008000h – 03FFFFh	224KB	Upper 7/8
1	X	1	1	1	NONE	NONE	NONE	NONE

Notes:
1. X = don’t care
2. L = Lower; U = Upper
3. If any Erase or Program Instruction specifies a memory region that contains a protected data portion, this Instruction will be ignored.

7.1.19 W25Q10RL Status Register Memory Protection (CMP = 0)

STATUS REGISTER[1]					W25Q10RL (1M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1	010000h – 01FFFFh	64KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/2
0	X	0	1	X	0 thru 1	000000h – 01FFFFh	128KB	ALL
0	X	1	X	X	0 thru 1	000000h – 01FFFFh	128KB	ALL
1	0	0	0	1	1	01F000h – 01FFFFh	4KB	Upper 1/32
1	0	0	1	0	1	01E000h – 01FFFFh	8KB	Upper 1/16
1	0	0	1	1	1	01C000h – 01FFFFh	16KB	Upper 1/8
1	0	1	0	0	1	018000h – 01FFFFh	32KB	Upper 1/4
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/32
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/16
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/8
1	1	1	0	0	0	000000h – 007FFFh	32KB	Lower 1/4
1	X	1	1	1	0 thru 1	000000h – 01FFFFh	128KB	ALL

Notes:
1. X = don’t care
2. L = Lower; U = Upper
3. If any Erase or Program Instruction specifies a memory region that contains a protected data portion, this Instruction will be ignored.

7.1.20 W25Q10RL Status Register Memory Protection (CMP = 1)

STATUS REGISTER[(1)]					W25Q10RL (1M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 1	000000h – 01FFFFh	128KB	ALL
0	0	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/2
0	1	0	0	1	1	010000h – 01FFFFh	64KB	Upper 1/2
0	X	0	1	X	NONE	NONE	NONE	NONE
0	X	1	X	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 1	000000h – 01EFFFh	124KB	Lower 31/32
1	0	0	1	0	0 thru 1	000000h – 01DFFFh	120KB	Lower 15/16
1	0	0	1	1	0 thru 1	000000h – 01BFFFh	112KB	Lower 7/8
1	0	1	0	0	0 thru 1	000000h – 017FFFh	96KB	Lower 3/4
1	1	0	0	1	0 thru 1	001000h – 01FFFFh	124KB	Upper 31/32
1	1	0	1	0	0 thru 1	002000h – 01FFFFh	120KB	Upper 15/16
1	1	0	1	1	0 thru 1	004000h – 01FFFFh	112KB	Upper 7/8
1	1	1	0	0	0 thru 1	008000h – 01FFFFh	96KB	Upper 3/4
1	X	1	1	1	NONE	NONE	NONE	NONE

Notes:

1. X = don’t care
2. L = Lower; U = Upper
3. If any Erase or Program Instruction specifies a memory region that contains a protected data portion, this Instruction will be ignored.

8. INSTRUCTIONS

The Standard/Dual/Quad SPI command set of the W25Q40/20/10RL consists of 48 basic commands that are fully controlled through the SPI bus (see Command Set Table1-2). Commands are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the command code. Data on the DI input is sampled on the rising edge of clock with the most significant bit (MSB) first.

The QPI Instruction set of the W25Q16RL consists of 35 basic Instructions that are fully controlled through the SPI bus (see Instruction Set Table 3). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through the IO[3:0] pins provides the Instruction code. Data on all four IO pins are sampled on the rising edge of clock with the most significant bit (MSB) first. All QPI Instructions, addresses, data and dummy bytes use all four IO pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of /CS. Clock relative timing diagrams for each Instruction are included in Figures 5 through 57. All read Instructions can be completed after any clocked bit. However, all Instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the Instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all Instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.1 Device ID and Command Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**	
Winbond Serial Flash	EFh	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Command	**ABh, 90h, 92h, 94h**	**9Fh**
W25Q40RL-M	12h	7013h
W25Q20RL-M	11h	7012h
W25Q10RL-M	10h	7011h

8.1.2 Command Set Table 1 (Standard SPI Commands) [(1)]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock$_{(1-1-1)}$	**8**	**8**	**8**	**8**	**8**	**8**	**8**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)[(2)]		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[(3)]	
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Chip Erase	**C7h/60h**						
Read Status Register-1	**05h**	(S7-S0)[(2)]					
Write Status Register-1	**01h**	(S7-S0)					
Read Status Register-2	**35h**	(S15-S8)[(2)]					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-S16)[(2)]					
Write Status Register-3	**11h**	(S23-S16)					
Read SFDP Register	**5Ah**	00	00	A7-A0	Dummy	(D7-D0)	
Erase Security Register[(4)]	**44h**	A23-A16	A15-A8	A7-A0			
Program Security Register[(4)]	**42h**	A23-A16	A15-A8	A7-A0	D7-D0[(3)]		
Read Security Register[(4)]	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Set Read Parameters	**C0h**	P7-P0					
Enter QPI Mode	**38h**						
Enable Reset	**66h**						
Reset Device	**99h**						

8.1.3 Command Set Table 2 (Dual/Quad SPI Commands)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)[6]	…	
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual I/O	**BBh**	A23-A16[5]	A15-A8[5]	A7-A0[5]	M7-M0	(D7-D0)[6]	…		
Mftr./Device ID Dual I/O	**92h**	A23-A16[5]	A15-A8[5]	00[5]	Dummy[13]	(MF7-MF0)	(ID7-ID0)[6]		
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)[8]	(D7-D0)[3]	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)[9]
Number of Clock(1-4-4)	**8**	**2**[7]	**2**[7]	**2**[7]	**2**	**2**	**2**	**2**	**2**
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	00	Dummy[13]	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy[11]	(D7-D0)	…
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				

8.1.4 Command Set Table 3 (QPI Commands)(10)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock (4-4-4)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read SFDP Register	**5Ah**	00	00	A7-A0	Dummy	(D7-D0)	
Set Read Parameters	**C0h**	P7-P0					
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0(8)	D7-D0(3)	…
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0			
Chip Erase	**C7h/60h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1	**01h**	(S7-S0)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-S16)(2)					
Write Status Register-3	**11h**	(S23-S16)					
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Enable Reset	**66h**						
Reset Device	**99h**						
Exit QPI Mode	**FFh**						
Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Number of Clock (4-4-4)	**2**	**2**	**2**	**2**	**2**	**4**	**2**
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy(11)	(D7-D0)
Burst Read with Wrap	**0Ch**	A23-A16	A15-A8	A7-A0	Dummy	Dummy(11)	(D7-D0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0(13)	Dummy(11)	(D7-D0)

8.1.5 Instruction Set Table 4 (DTR with SPI Instructions)

Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Number of Clock(1-1-1)	8	4	4	4	6	4	4
DTR Fast Read	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock(1-2-2)	8	2	2	2	2	4	2
DTR Fast Read Dual I/O	**BDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)
Number of Clock(1-4-4)	8	1	1	1	1	7	1
DTR Fast Read Quad I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

8.1.6 Instruction Set Table 5 (DTR with QPI Instructions)

Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Number of Clock (4-4-4)	2	1	1	1	8	1	1
DTR Read with Wrap(13)	**0Eh**	A23-A16	A15-A8	A7-0	Dummy	(D7-D0)	…
DTR Fast Read I/O	**0Dh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock (4-4-4)	2	1	1	1	1	7	1
DTR Fast Read I/O	**EDh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Notes:

1. Data bytes are shifted with the Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data is output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and the Device ID will repeat continuously until /CS terminates the Instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers. Up to 256 bytes of data can be input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte addressl
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
5. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
6. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
7. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
8. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
9. Fast Read Quad I/O data output format:
   IO0 = (x, x, x, x, D4, D0, D4, D0)
   IO1 = (x, x, x, x, D5, D1, D5, D1)
   IO2 = (x, x, x, x, D6, D2, D6, D2)
   IO3 = (x, x, x, x, D7, D3, D7, D3)
10. QPI Instruction, Address, Data input/output format:
    CLK # 0 1 2 3 4 5 6 7 8 9 10 11
    IO0 = C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0
    IO1 = C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1
    IO2 = C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2
    IO3 = C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3
11. The number of dummy clocks for QPI/SPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
12. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.
13. If not using the Read Command Bypass Mode, the first dummy byte is M7-M0 should be set to Fxh,

8.2 Command Descriptions

8.2.1 Write Enable (06h)

The Write Enable command (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers command. The Write Enable command is entered by driving /CS low, shifting the command code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

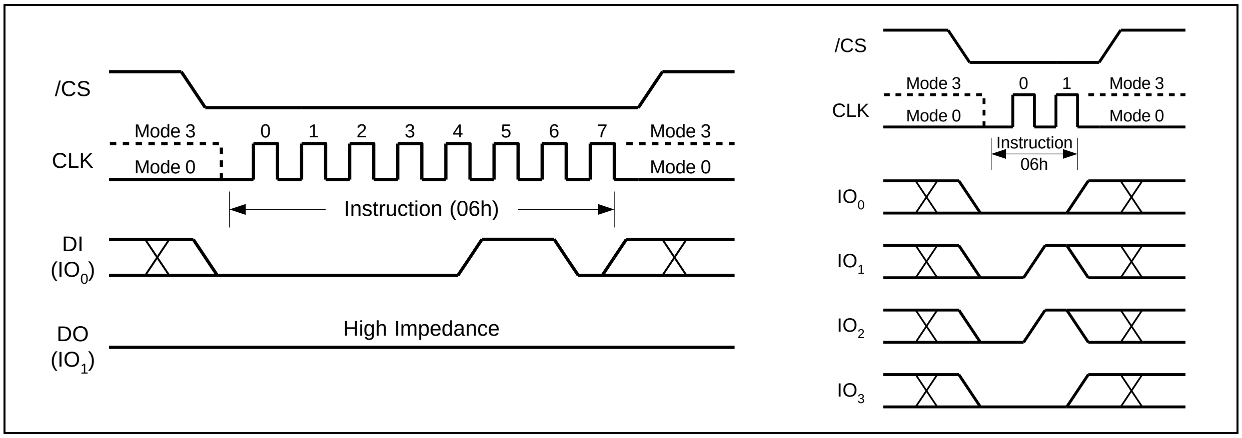


Figure 5. Write Enable Command for SPI Mode (left) or QPI Mode (right)

8.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) Instruction must be issued prior to a Write Status Register (01h) Instruction. The Write Enable for Volatile Status Register Instruction (Figure 6) will not set the Write Enable Latch (WEL) bit and it is only valid for the Write Status Register Instruction to change the volatile Status Register bit values.

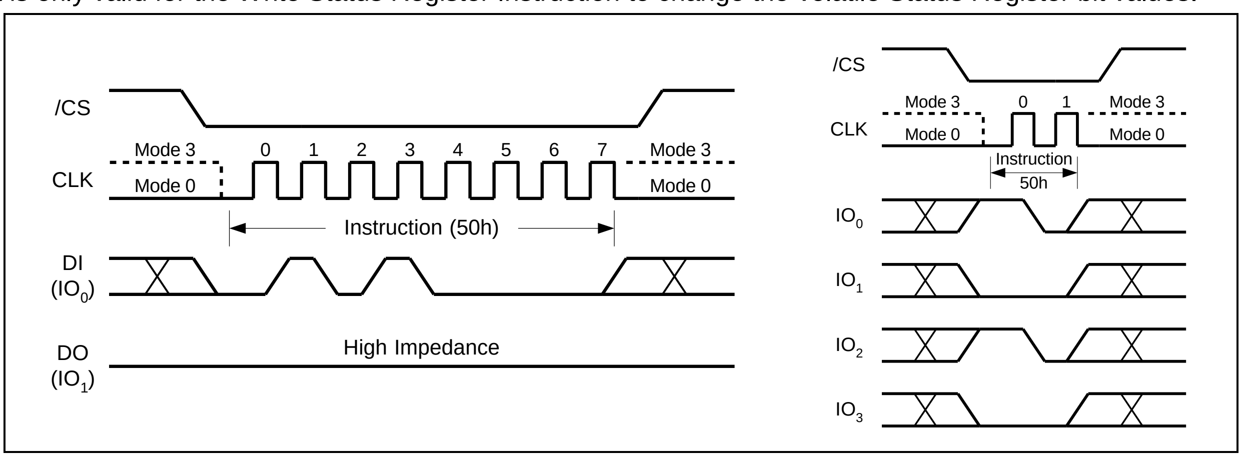


Figure 6. Write Enable for Volatile Status Register Command for SPI Mode (left) or QPI Mode (right)

8.2.3 Write Disable (04h)

The Write Disable command (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable command is entered by driving /CS low, shifting the command code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset commands.

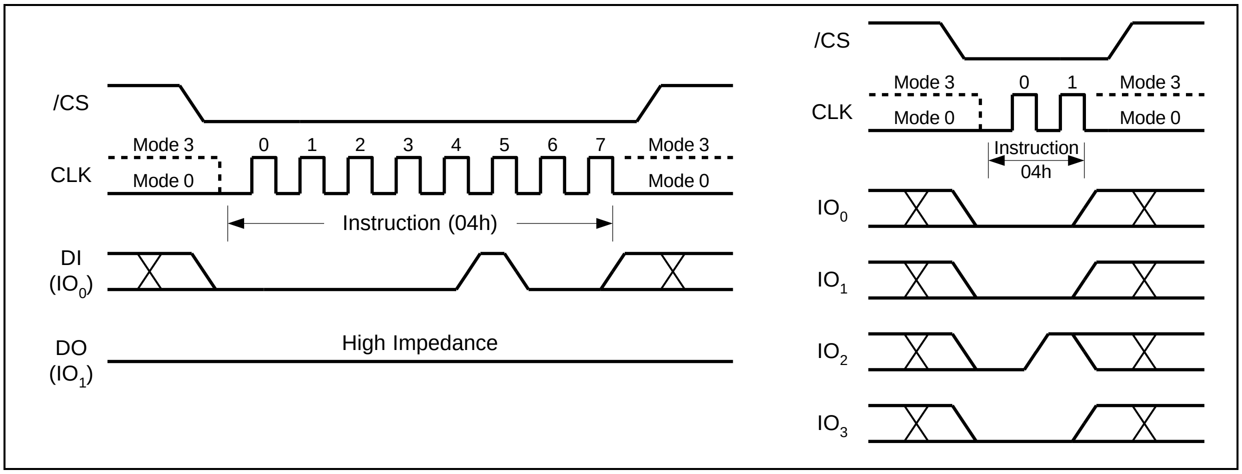


Figure 7. Write Disable Command for SPI Mode (left) or QPI Mode (right)

8.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register Instructions allow the 8-bit Status Registers to be read. The Instruction is entered by driving /CS low and shifting the Instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 8. Refer to section 7.1 for Status Register descriptions.

The Read Status Register Instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another Instruction. The Status Register can be read continuously, as shown in Figure 8. The Instruction is completed by driving /CS high.

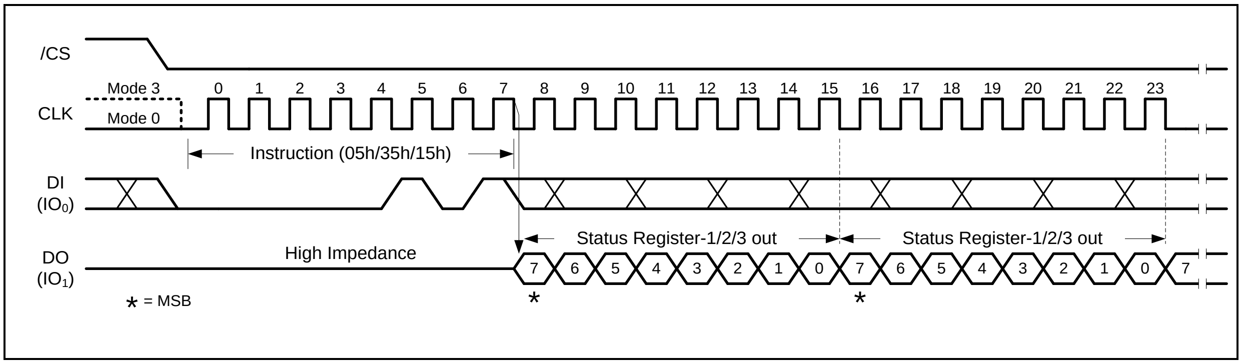


Figure 8a. Read Status Register Command (SPI Mode)

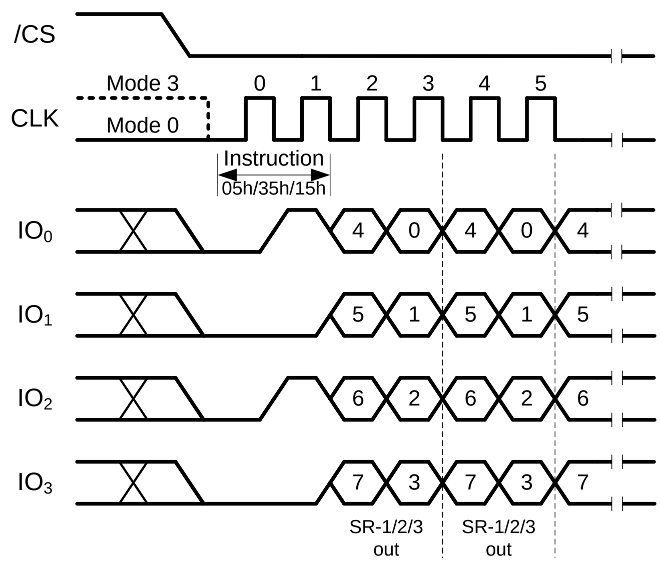


Figure 8b. Read Status Register Command (QPI Mode)

8.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register Instruction allows the Status Registers to be written. The writable Status Register bits include: SRP, SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; HOLD/RST, DRV1, DRV0 in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register Instruction. LB[3:1] are non-volatile OTP bits Once the bits are set to 1, they cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) Instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the Instruction is entered by driving /CS low, sending the Instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 9a & 9b.

To write the volatile Status Register bits, a Write Enable for Volatile Status Register (50h) Instruction must have been executed prior to the Write Status Register Instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During the non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register Instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other Instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During the volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See AC Characteristics). The BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register command can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to section 7.1 for Status Register descriptions.

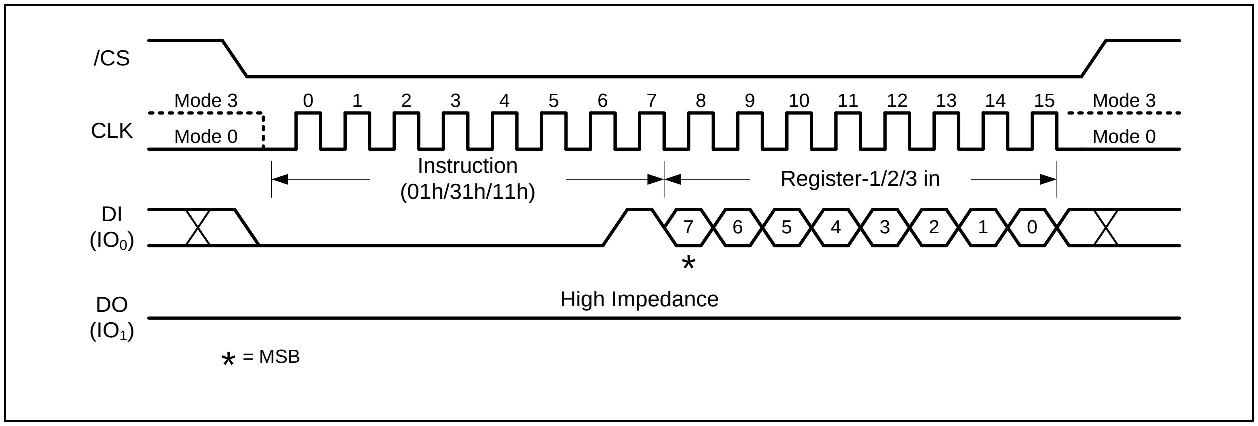


Figure 9a. Write Status Register-1/2/3 Command (SPI Mode)

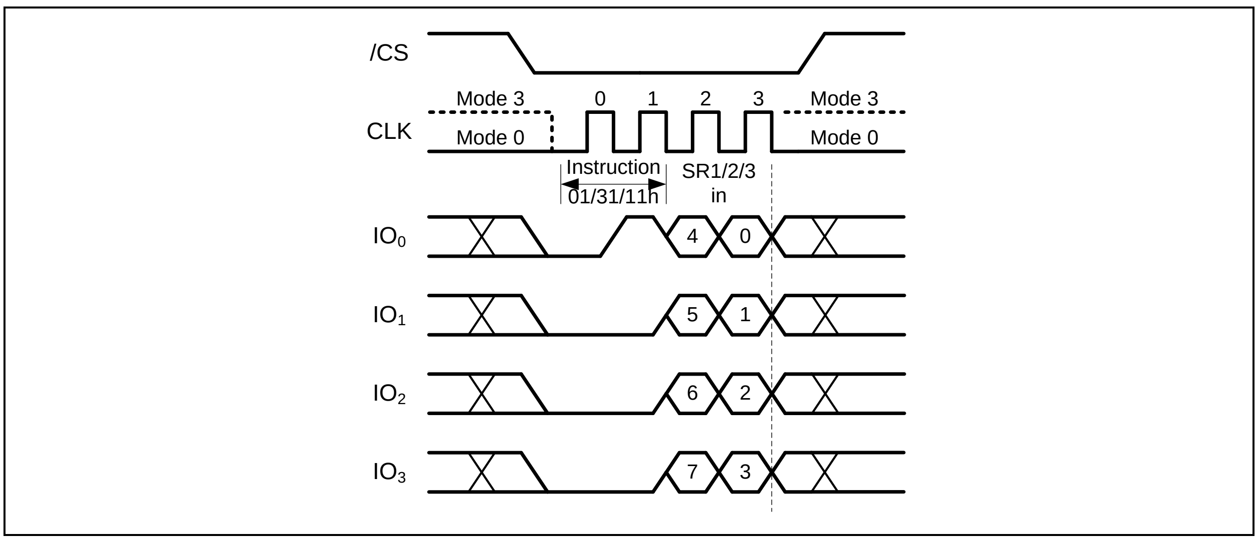


Figure 9b. Write Status Register-1/2/3 Command (QPI Mode)

8.2.6 Read Data (03h)

The Read Data command allows one or more data bytes to be sequentially read from the memory. The command is initiated by driving the /CS pin low and then shifting the command code "03h" followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving /CS high.

The Read Data command sequence is shown in Figure 14. If a Read Data command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle. The Read Data command allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data (03h) command is only supported in Standard SPI mode.

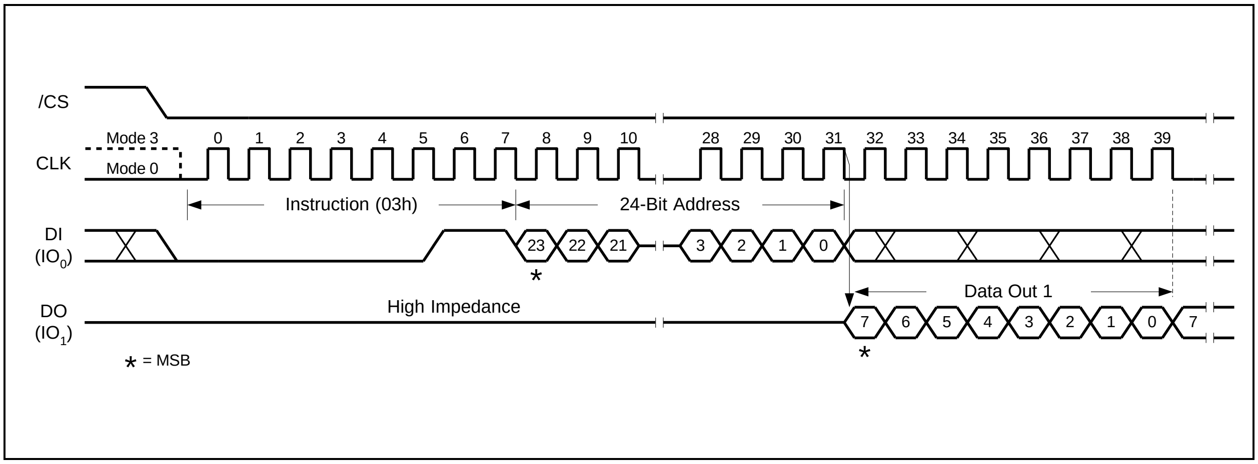


Figure 14. Read Data Command (SPI Mode only)

8.2.7 Fast Read (0Bh)

The Fast Read Instruction is similar to the Read Data Instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 16. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a "don't care".

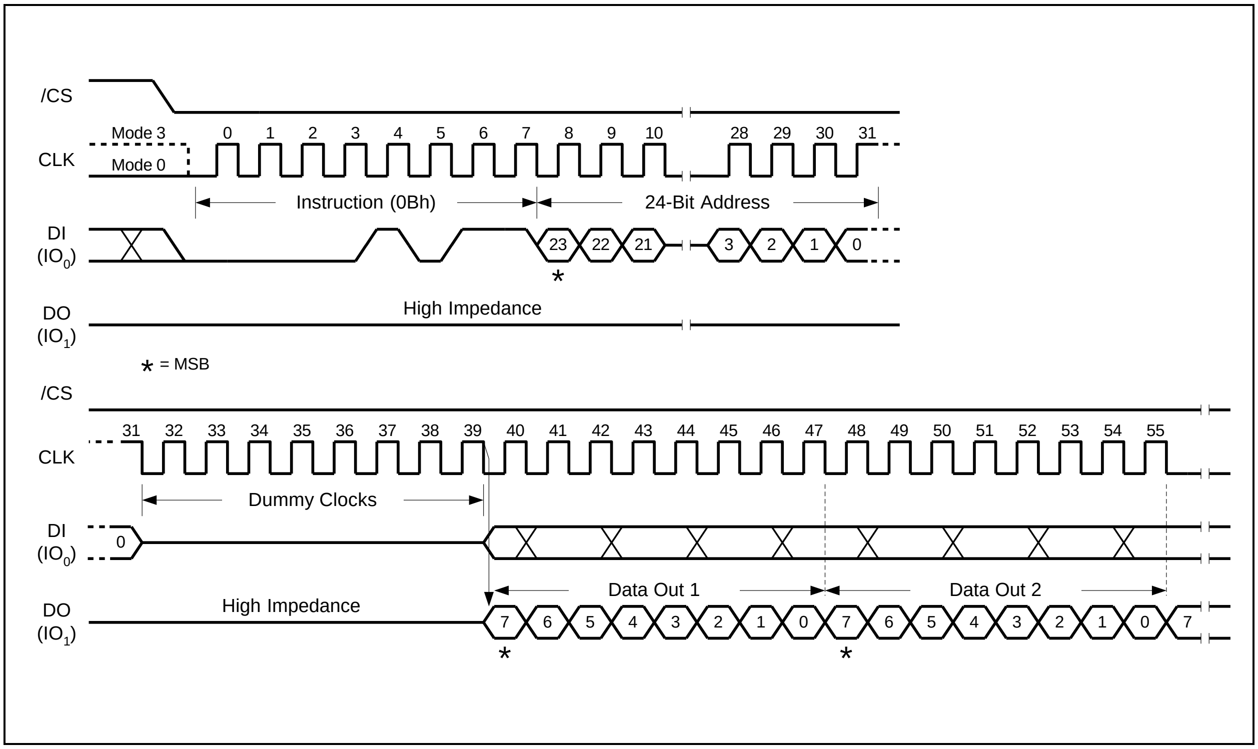


Figure 16a. Fast Read Command (SPI Mode)

Fast Read (0Bh) in QPI Mode

The Fast Read command is also supported in QPI mode. When the QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12, 14 or 16. The default number of dummy clocks upon power up or after a Reset command is 6.

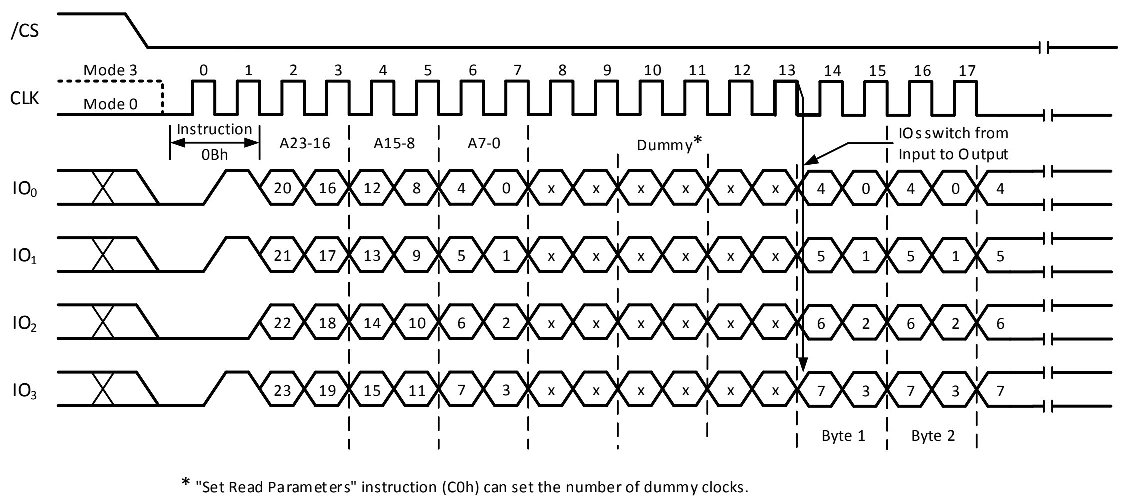


Figure 16b. Fast Read Command (QPI Mode)

8.2.8 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24-bit address as shown in Figure 17. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

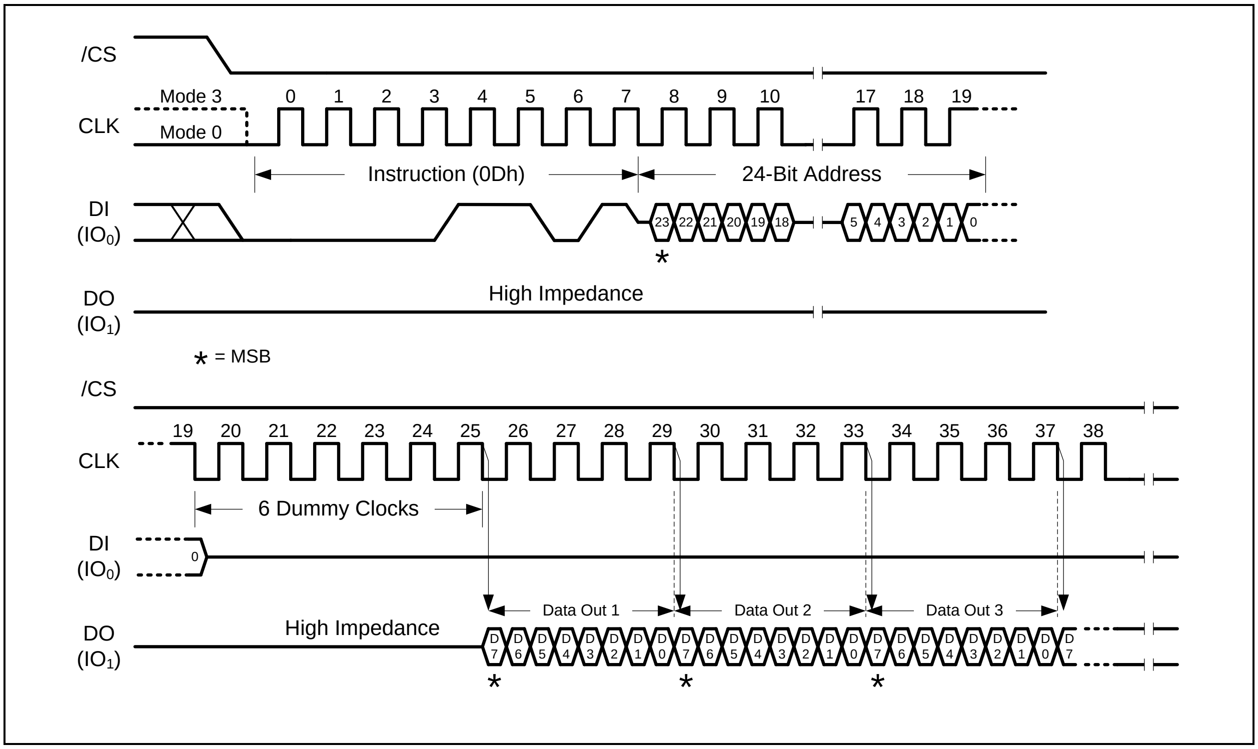


Figure 17a. DTR Fast Read Instruction (SPI Mode)

DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

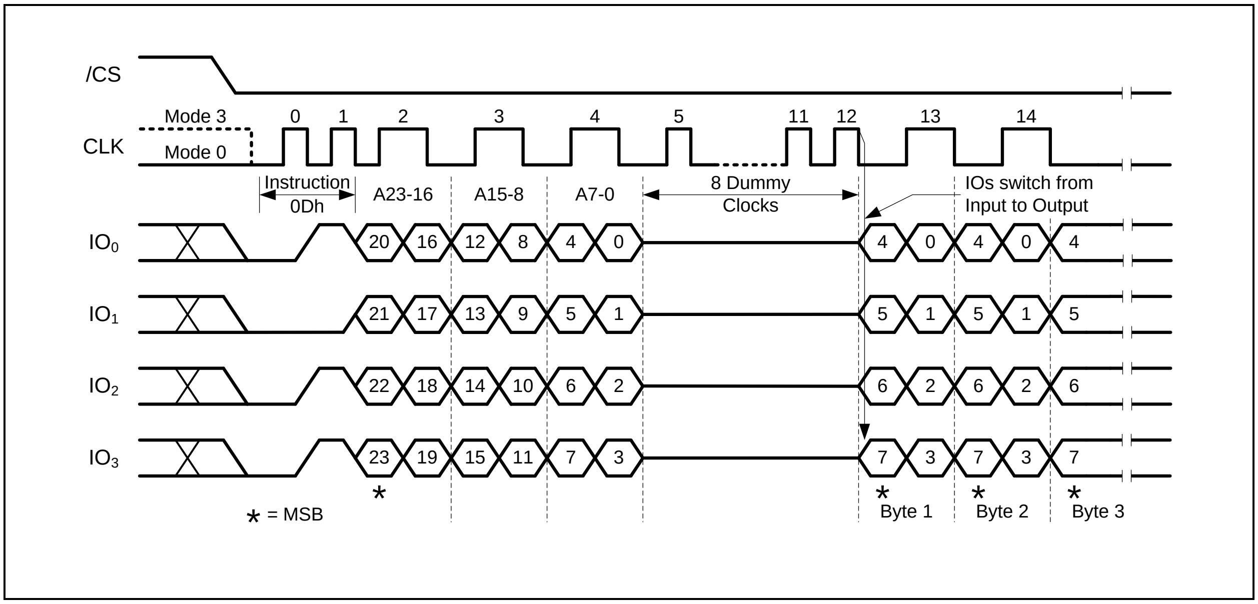


Figure 17b. DTR Fast Read Instruction (QPI Mode)

8.2.10 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) command is similar to the standard Fast Read (0Bh) command except that data is output on two pins; IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read command, the Fast Read Dual Output command can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 18. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO_0 pin should be high-impedance prior to the falling edge of the first data out clock.

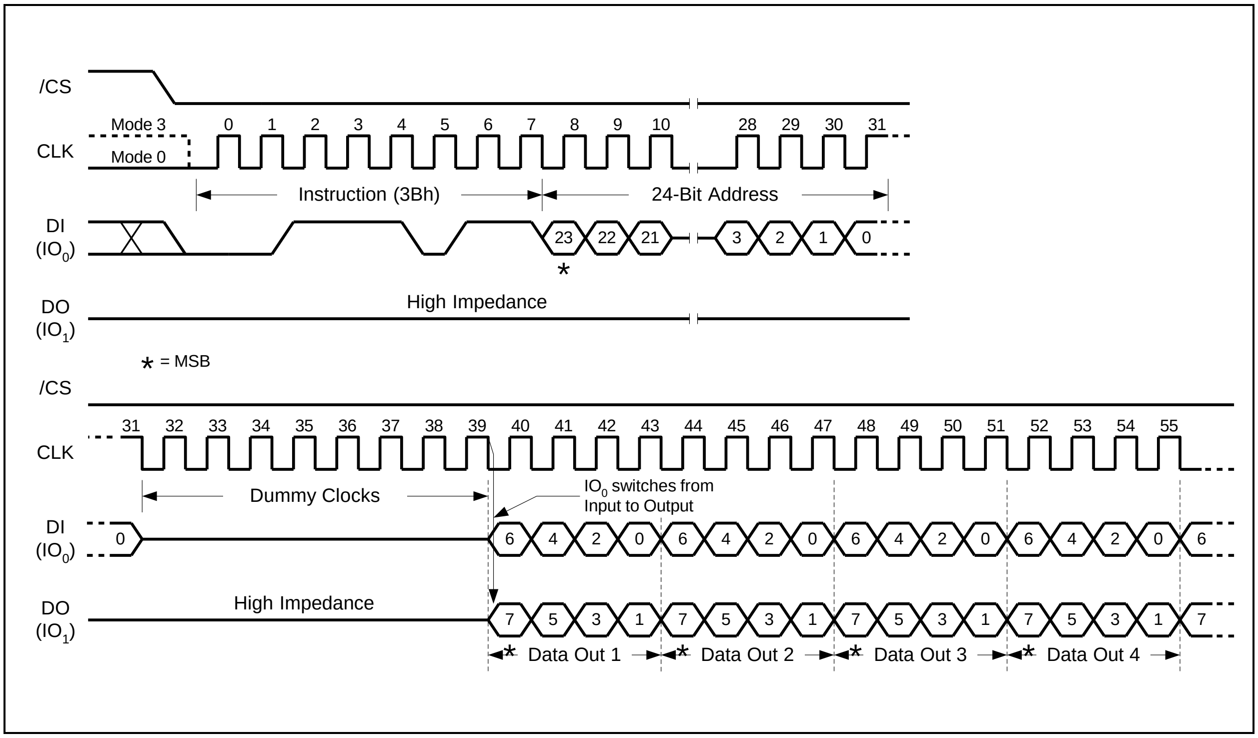


Figure 18. Fast Read Dual Output Command (SPI Mode only)

8.2.11 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) command is similar to the Fast Read Dual Output (3Bh) command except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Command. The Fast Read Quad Output Command allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output command can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 20. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

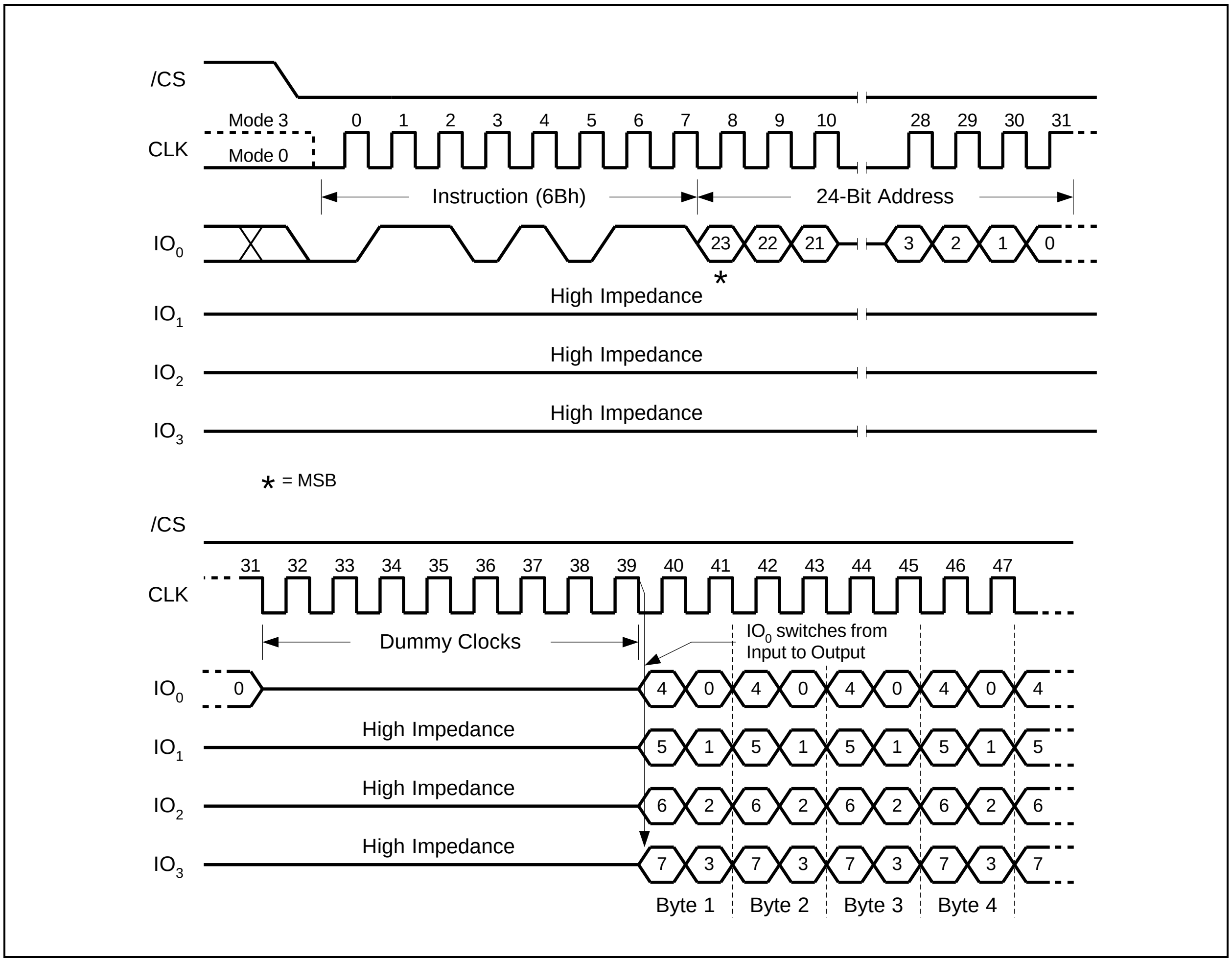


Figure 20. Fast Read Quad Output Command (SPI Mode only)

8.2.12 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) command allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) command but with the capability to input the Address bits (A23-0) two bits per clock. This reduced command overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Read Command Bypass Mode"

The Fast Read Dual I/O command can further reduce command overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 22a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O command (after /CS is raised and then lowered) does not require the BBh command code, as shown in Figure 22b. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next command (after /CS is raised and then lowered) requires the first byte command code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next command (16 clocks), to ensure M4 = 1 and return the device to normal operation.

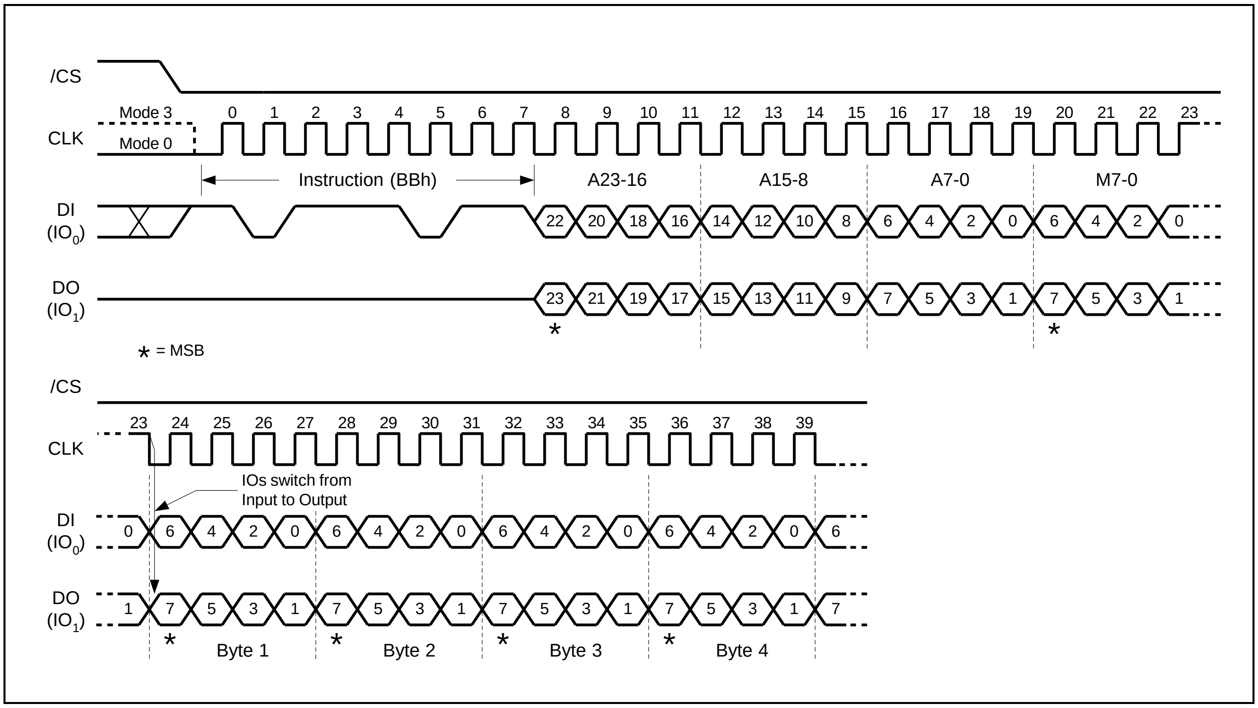


Figure 22a. Fast Read Dual I/O Command (Initial command or previous M5-4 ≠ 10, SPI Mode only)

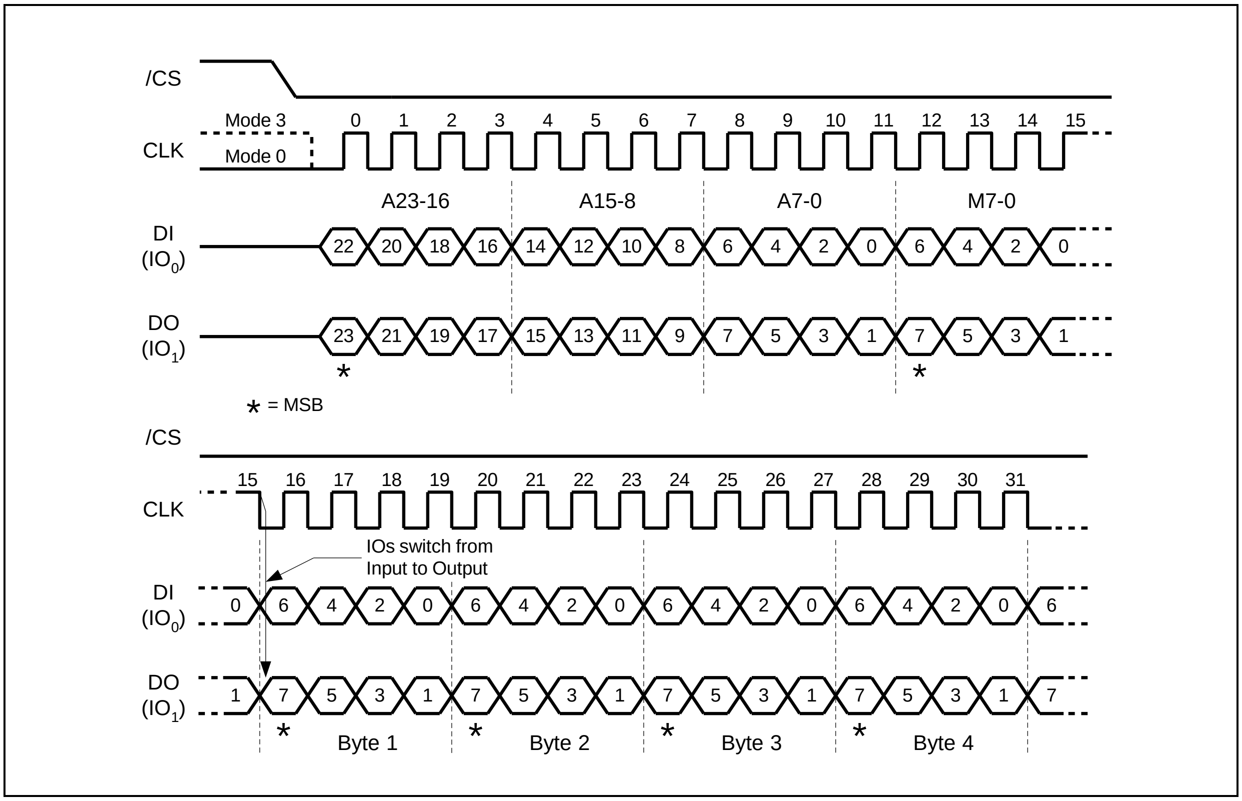


Figure 22b. Fast Read Dual I/O Command (Previous command set M5-4 = 10, SPI Mode only)

8.2.14 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Read Command Bypass Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 23a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 23b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh/FFFFFh on IO0 for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

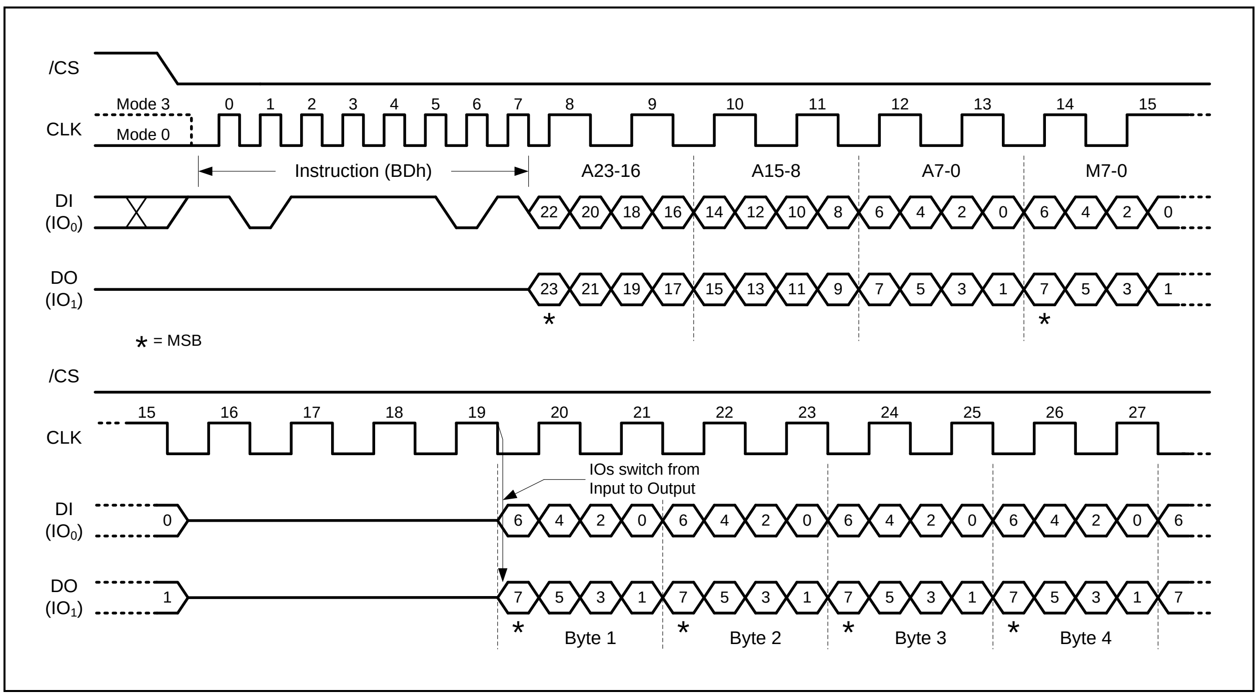


Figure 23a. DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

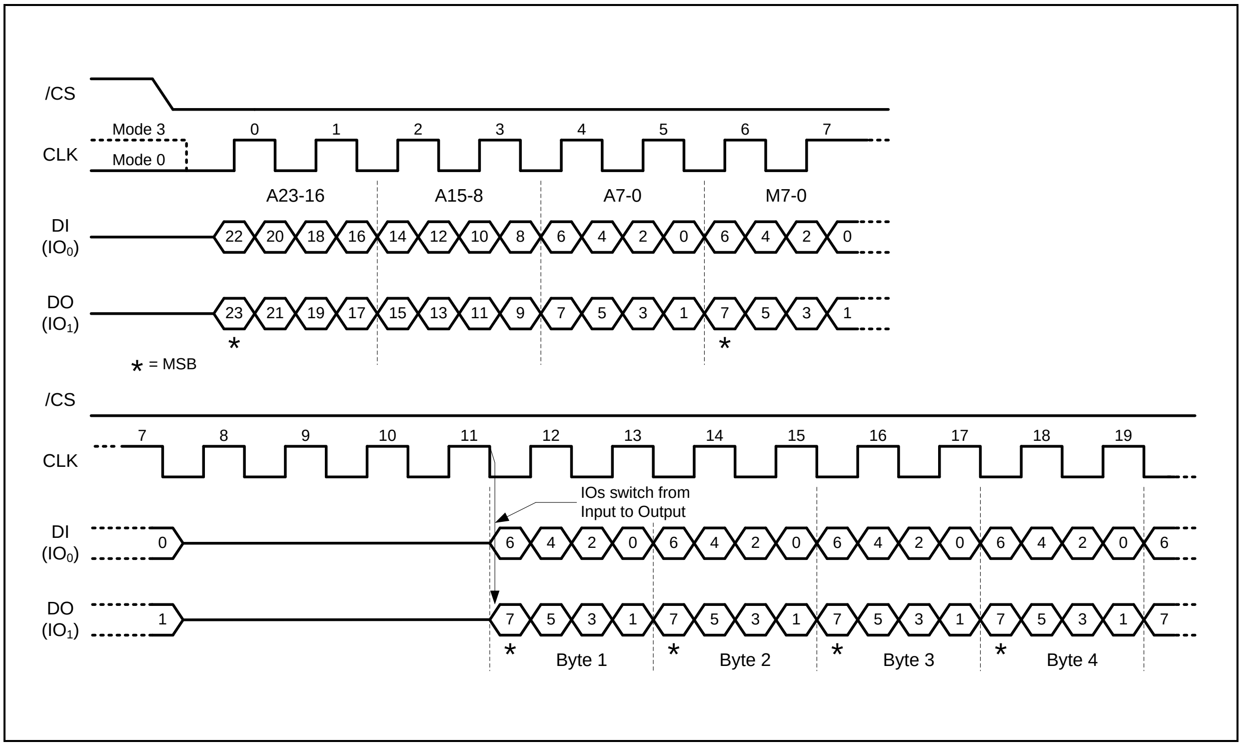


Figure 23b. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)

8.2.15 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) command is similar to the Fast Read Dual I/O (BBh) command except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces command overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Command.

The number of dummy clocks is configured by the "Set Read Parameters (C0h)" command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12, 14, or 16. The default number of dummy clocks upon power up or after a Reset command is 6. In SPI mode, the "Read Command Bypass Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

Fast Read Quad I/O with "Read Command Bypass Mode"

The Fast Read Quad I/O command can further reduce command overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 24a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after /CS is raised and then lowered) does not require the EBh command code, as shown in Figure 24b. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next command (after /CS is raised and then lowered) requires the first byte command code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next command (8 clocks), to ensure M4 = 1 and return the device to normal operation.

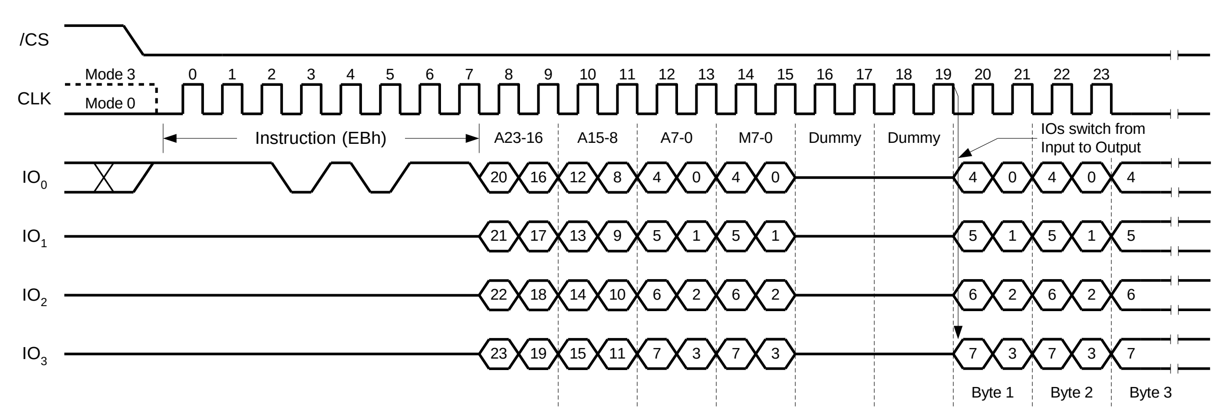


Figure 24a. Fast Read Quad I/O Command (Initial command or previous M5-4≠10, SPI Mode).

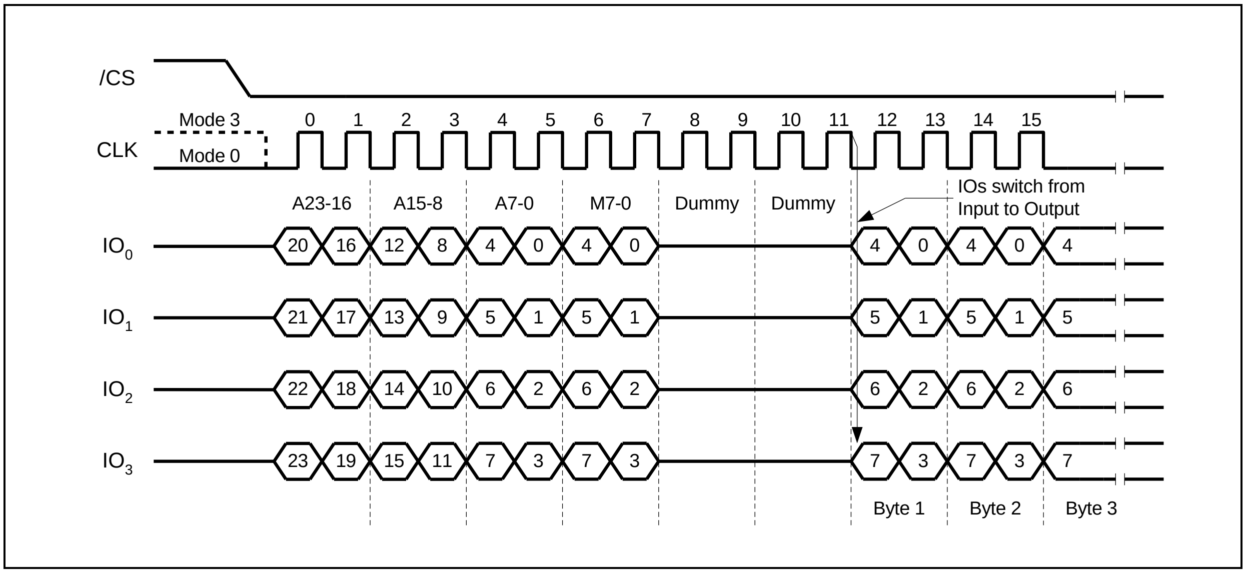


Figure 24b. Fast Read Quad I/O Command (Previous command set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Fast Read Quad I/O Instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) Instruction prior to EBh. The “Set Burst with Wrap” (77h) Instruction can either enable or disable the “Wrap Around” feature for the following EBh Instructions. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the Instruction Once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the Instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read Instructions.

The “Set Burst with Wrap” Instruction allows the three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while bits W6-5 are used to specify the length of the wrap around section within a page. Refer to “Set Burst with Wrap(77h)” for detail descriptions.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O command is also supported in QPI mode, as shown in Figure 24c. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12 or 16. The default number of dummy clocks upon power up or after a Reset command is 6. In QPI mode, the “Read Command Bypass Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

“Read Command Bypass Mode” feature is also available in QPI mode for Fast Read Quad I/O command. Please refer to the description on previous pages.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) command must be used. Please refer to “Burst Read with Wrap” (0Ch)” for details.

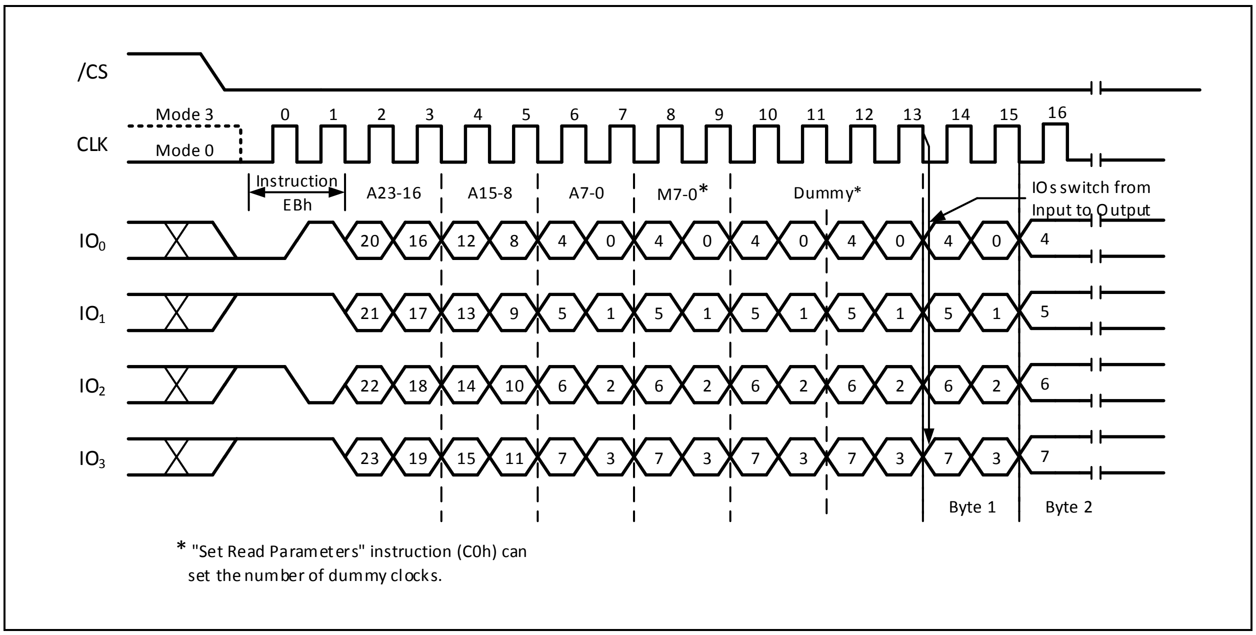


Figure 24c. Fast Read Quad I/O Command (Initial command or previous M5-4≠10, QPI Mode)
"Set Read Parameters" command (C0h) can set the number of dummy clocks.

8.2.16 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

DTR Fast Read Quad I/O with "Read Command Bypass Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Read Command Bypass Mode" bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure 24a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Read Command Bypass Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 24b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Read Command Bypass Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

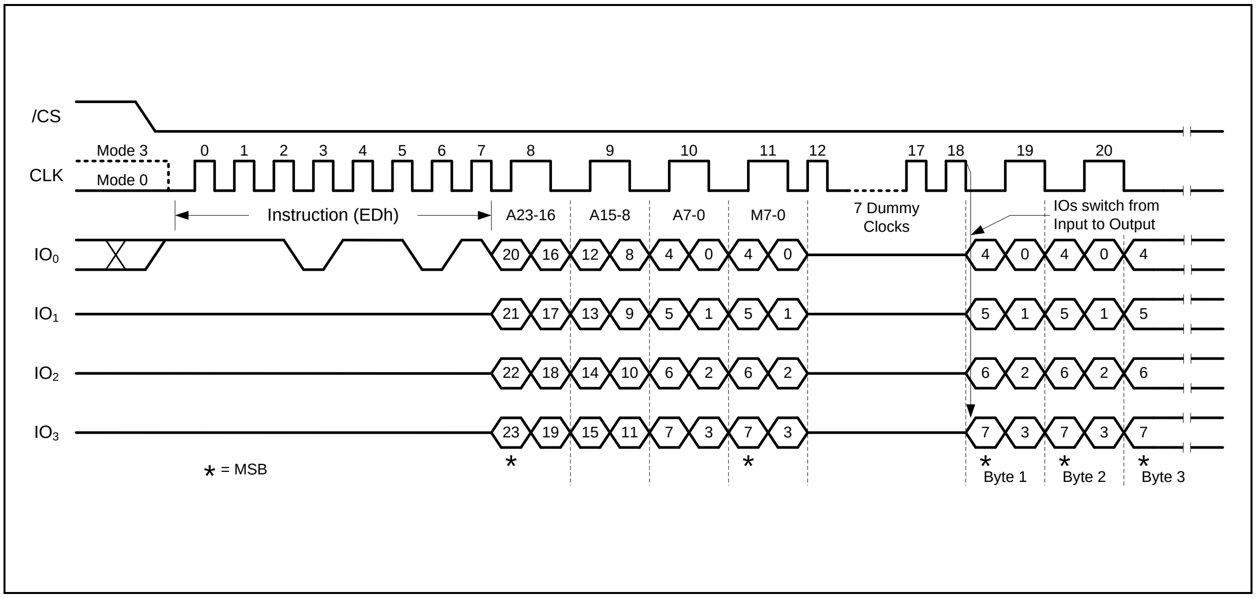


Figure 24a. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)

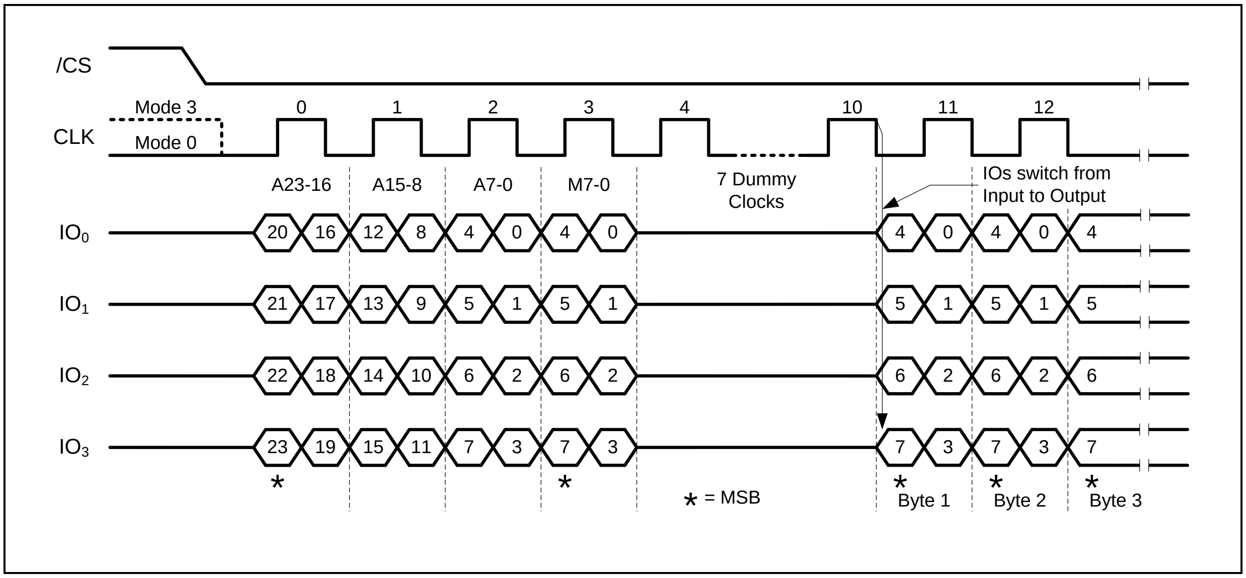


Figure 24b. Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)

DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to "Set Burst with Wrap(77h)" for detail descriptions.

DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 24c. In QPI mode, the “Read Command Bypass Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

“Read Command Bypass Mode” feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used. Please refer to “Burst Read with Wrap” (0Ch)” for details.

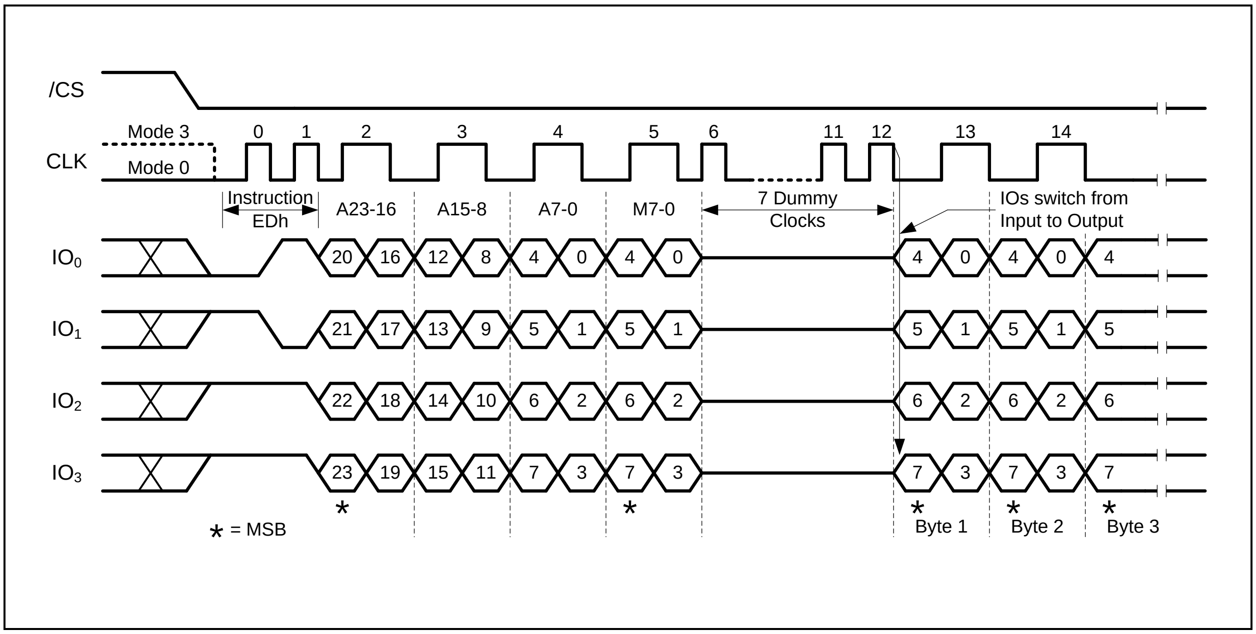


Figure 24c. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)

8.2.17 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) command is used in conjunction with "Fast Read Quad I/O" commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O command, the Set Burst with Wrap command is initiated by driving the /CS pin low and then shifting the command code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The command sequence is shown in Figure 28. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap command, the following "Fast Read Quad I/O" commands will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the "Burst Read with Wrap (0Ch)" command should be used to perform the Read operation with "Wrap Around" feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0h)" command. Refer to "Set Read Parameters (C0h)" and "Burst Read with Wrap" (0Ch)" for details.

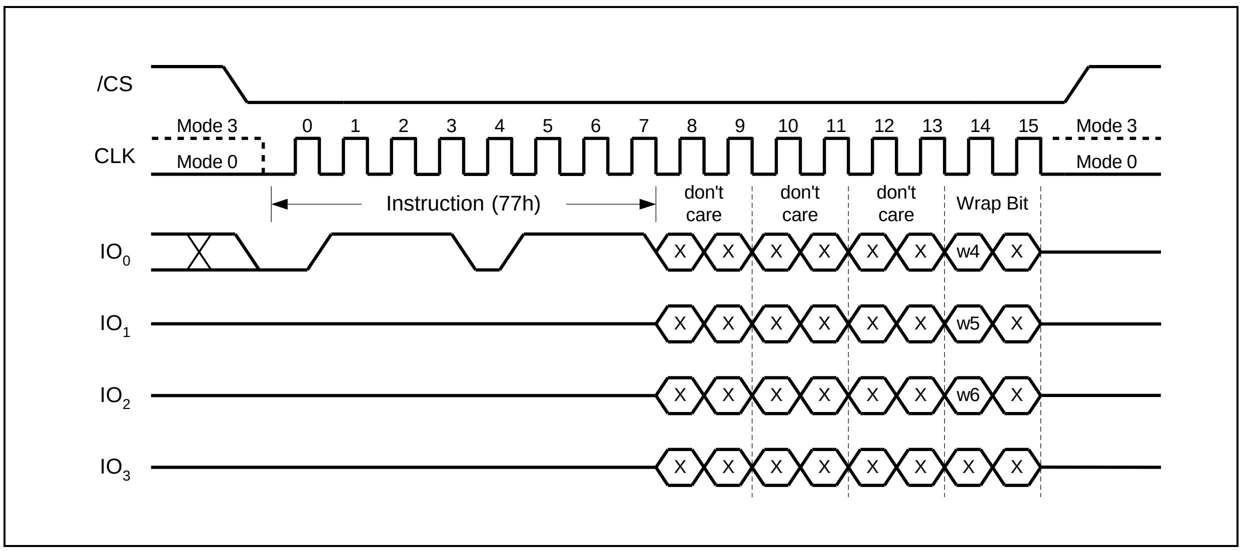


Figure 28. Set Burst with Wrap Command (SPI Mode only)

8.2.18 Page Program (02h)

The Page Program command allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Page Program Command (Status Register bit WEL= 1). The command is initiated by driving the /CS pin low then shifting the command code "02h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the command while data is being sent to the device. The Page Program command sequence is shown in Figure 29.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase commands, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command will not be executed. After /CS is driven high, the self-timed Page Program command will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

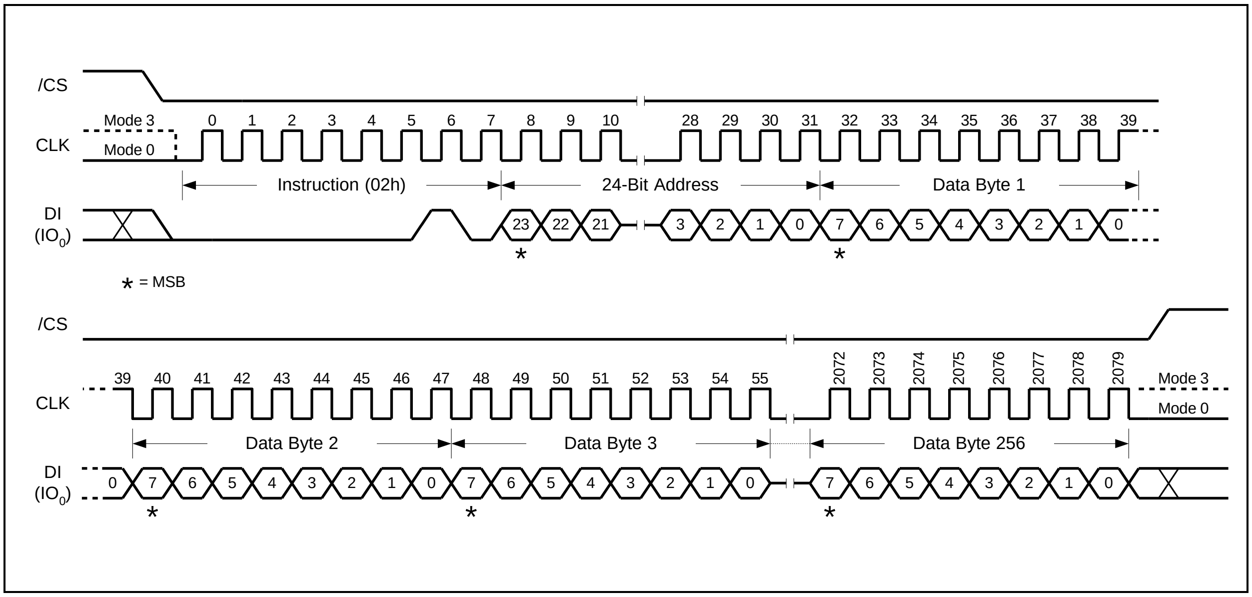


Figure 29a. Page Program Command (SPI Mode)

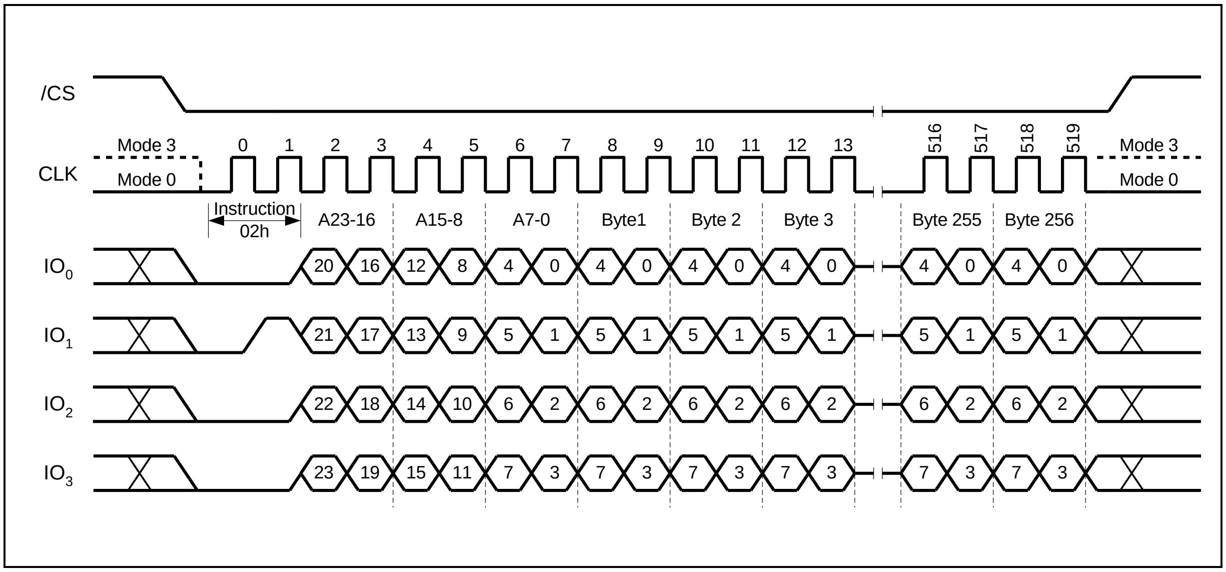


Figure 29b. Page Program Command (QPI Mode)

8.2.19 Quad Input Page Program (32h)

The Quad Page Program command allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO_0, IO_1, IO_2, and IO_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program command since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable command must be executed before the device will accept the Quad Page Program command (Status Register-1, WEL=1). The command is initiated by driving the /CS pin low then shifting the command code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the command while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program command sequence is shown in Figure 30.

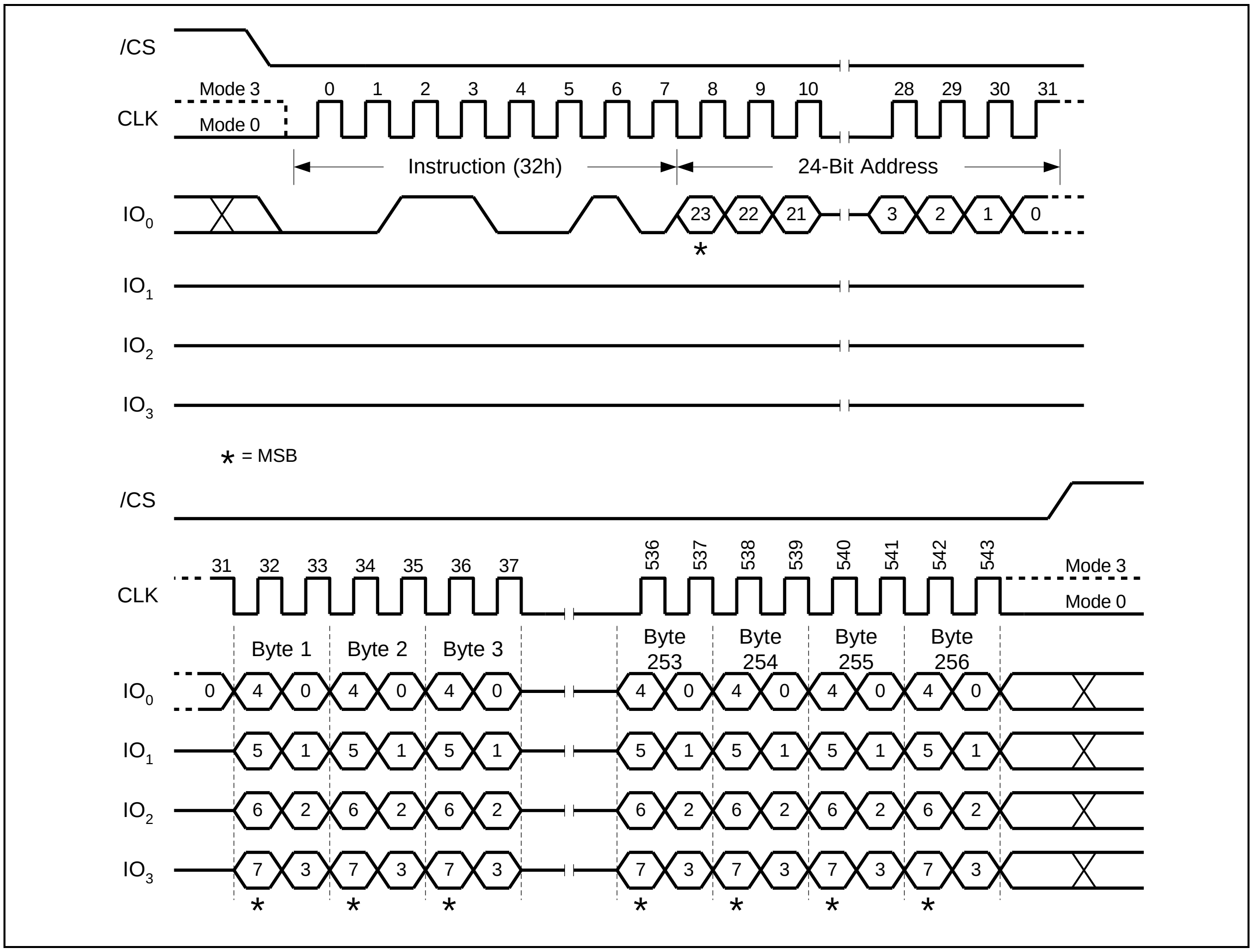


Figure 30. Quad Input Page Program Command (SPI Mode only)

Publication Release Date: February 18, 2025
-Revision D

8.2.20 Sector Erase (20h)

The Sector Erase command sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Sector Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the /CS pin low and shifting the command code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase command sequence is shown in Figure 31a & 31b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase command will not be executed. After /CS is driven high, the self-timed Sector Erase command will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

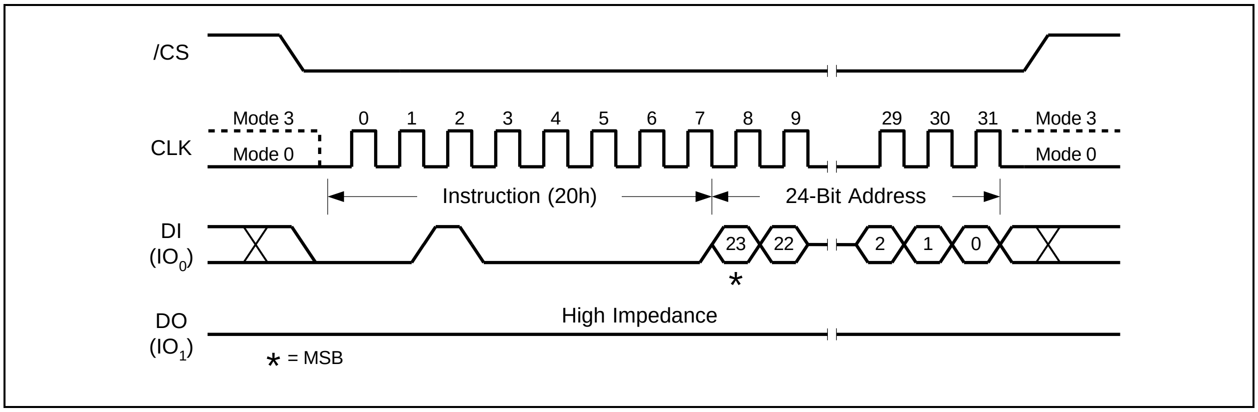


Figure 31a. Sector Erase Command (SPI Mode)

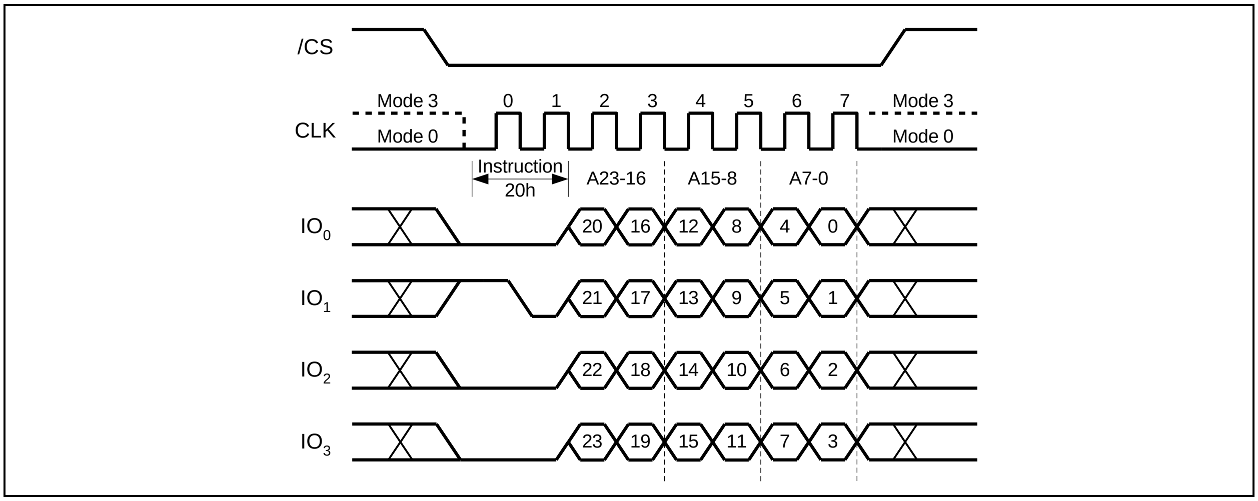


Figure 31b. Sector Erase Command (QPI Mode)

8.2.21 32KB Block Erase (52h)

The Block Erase command sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the /CS pin low and shifting the command code "52h" followed a 24-bit block address (A23-A0). The Block Erase command sequence is shown in Figure 32a & 32b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After /CS is driven high, the self-timed Block Erase command will commence for a time duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

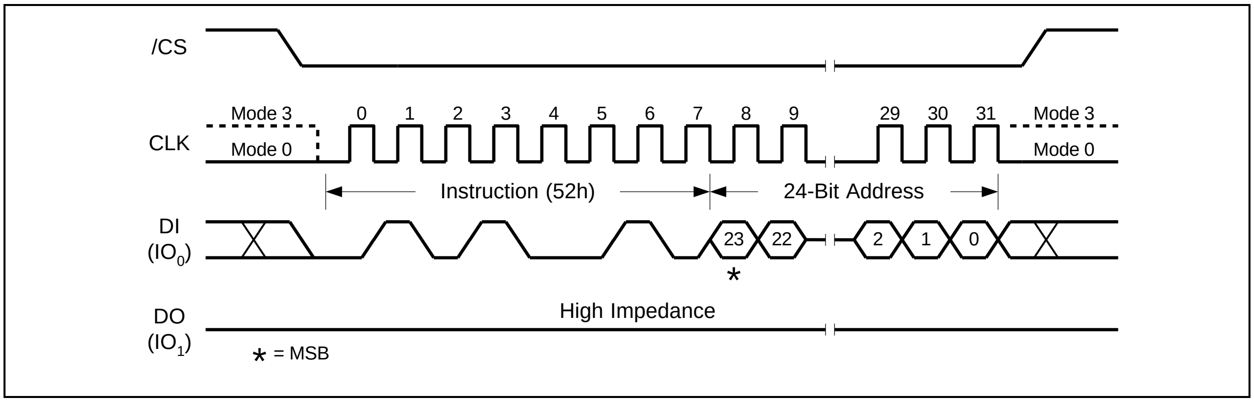


Figure 32a. 32KB Block Erase Command (SPI Mode)

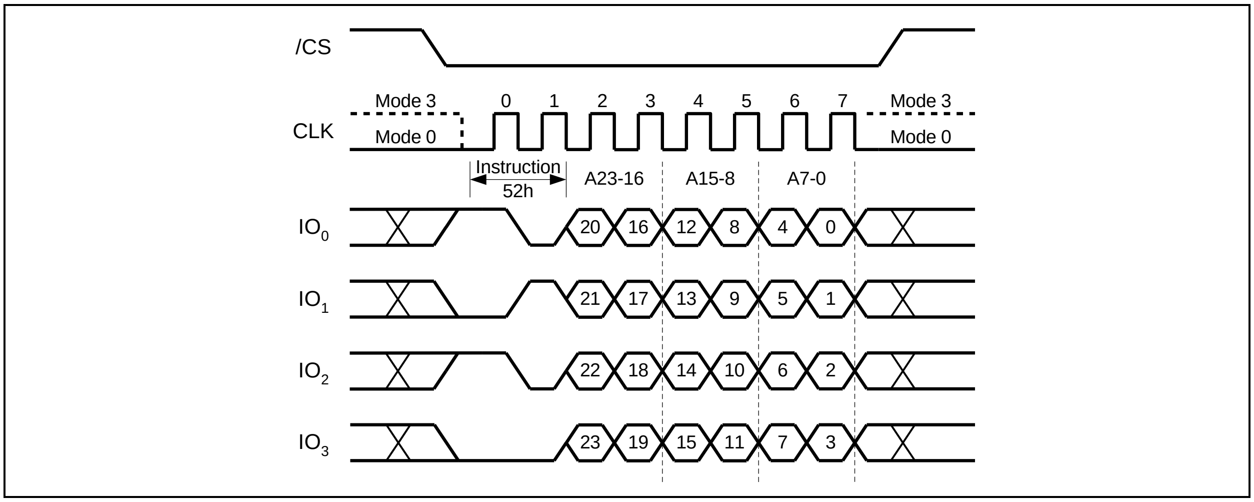


Figure 32b. 32KB Block Erase Command (QPI Mode)

8.2.22 64KB Block Erase (D8h)

The Block Erase command sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the /CS pin low and shifting the command code "D8h" followed a 24-bit block address (A23-A0). The Block Erase command sequence is shown in Figure 33a & 33b.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After /CS is driven high, the self-timed Block Erase command will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

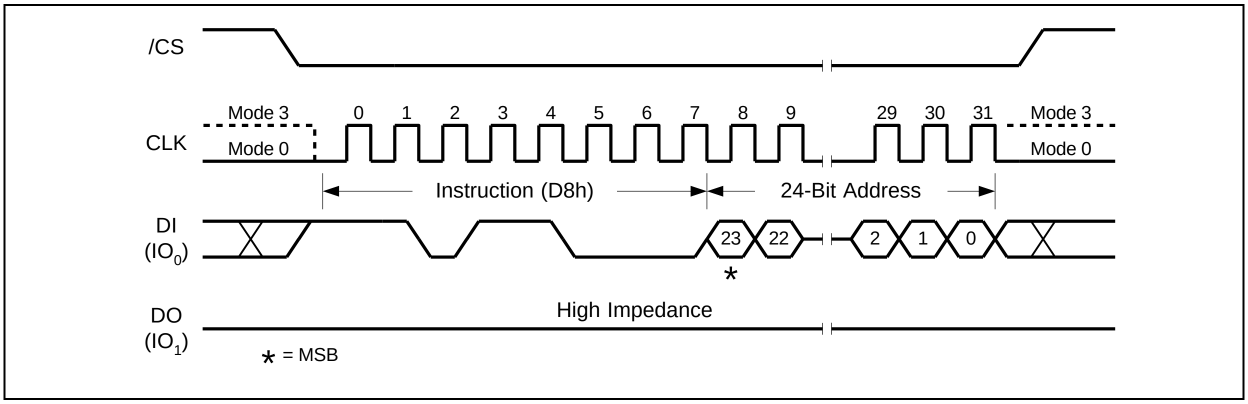


Figure 33a. 64KB Block Erase Command (SPI Mode)

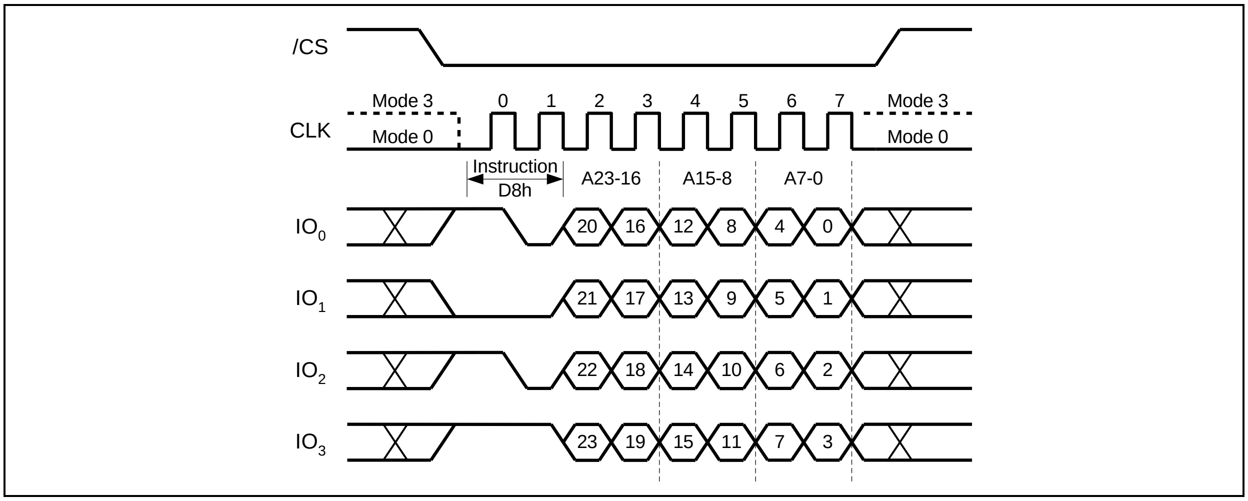


Figure 33b. 64KB Block Erase Command (QPI Mode)

8.2.23 Chip Erase (C7h / 60h)

The Chip Erase command sets all memory within the device to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Chip Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the /CS pin low and shifting the command code "C7h" or "60h". The Chip Erase command sequence is shown in Figure 34.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command will not be executed. After /CS is driven high, the self-timed Chip Erase command will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

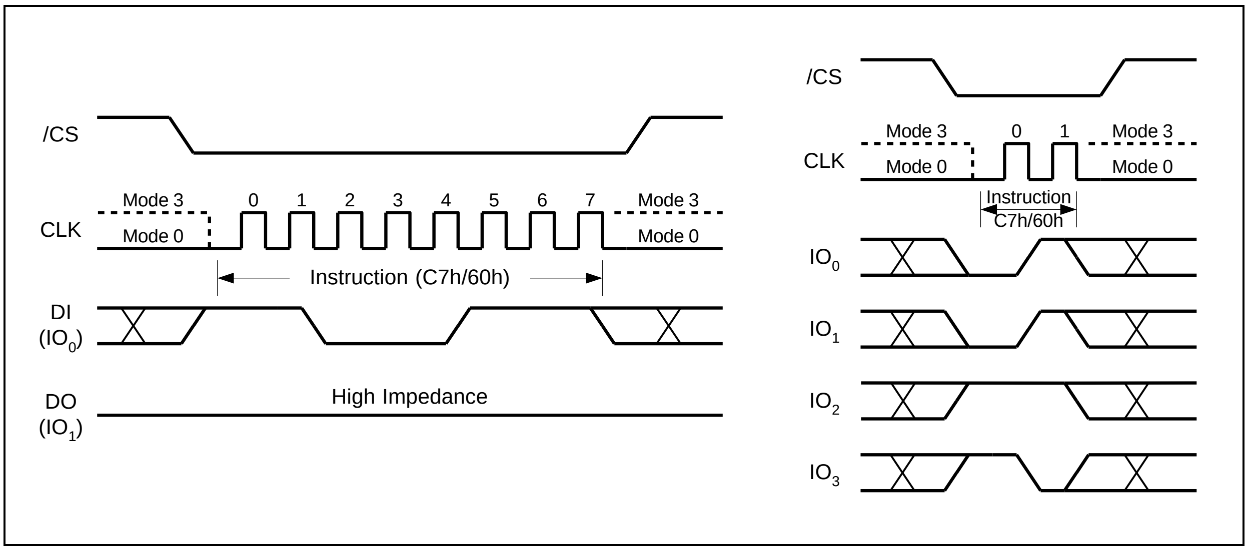


Figure 34. Chip Erase Command for SPI Mode (left) or QPI Mode (right)

8.2.24 Erase / Program Suspend (75h)

The Erase/Program Suspend command “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend command sequence is shown in Figure 35a & 35b.

The Write Status Register command (01h) and Erase commands (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend command is ignored. The Write Status Register command (01h) and Program commands (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend command “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend command will be ignored by the device. A maximum of time of “t_{SUS}” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend command “75h” is not issued earlier than a minimum of time of “t_{SUS}” following the preceding Resume command “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

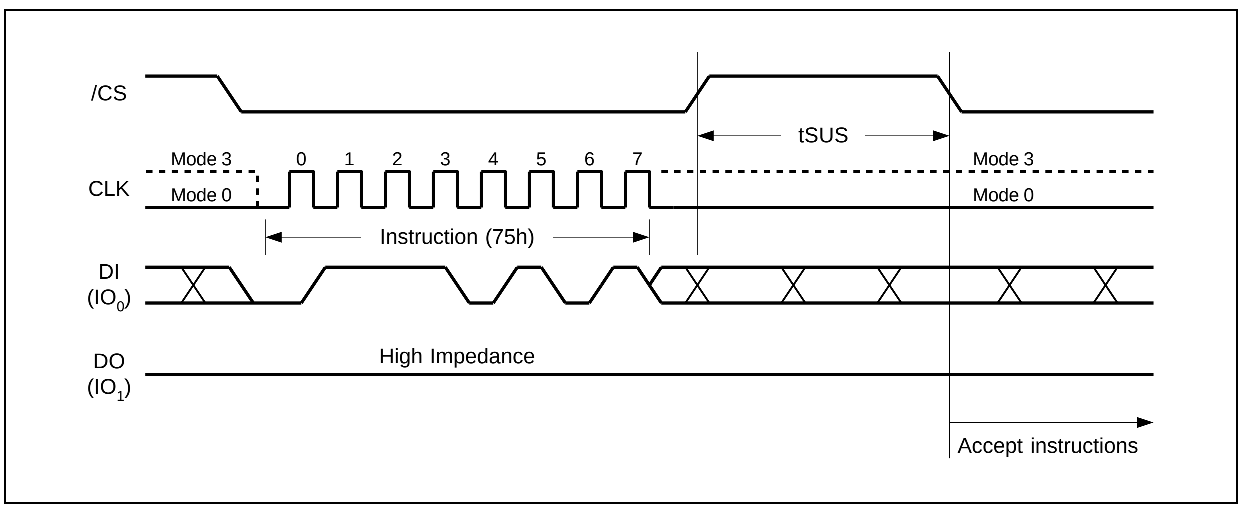


Figure 35a. Erase/Program Suspend Command (SPI Mode)

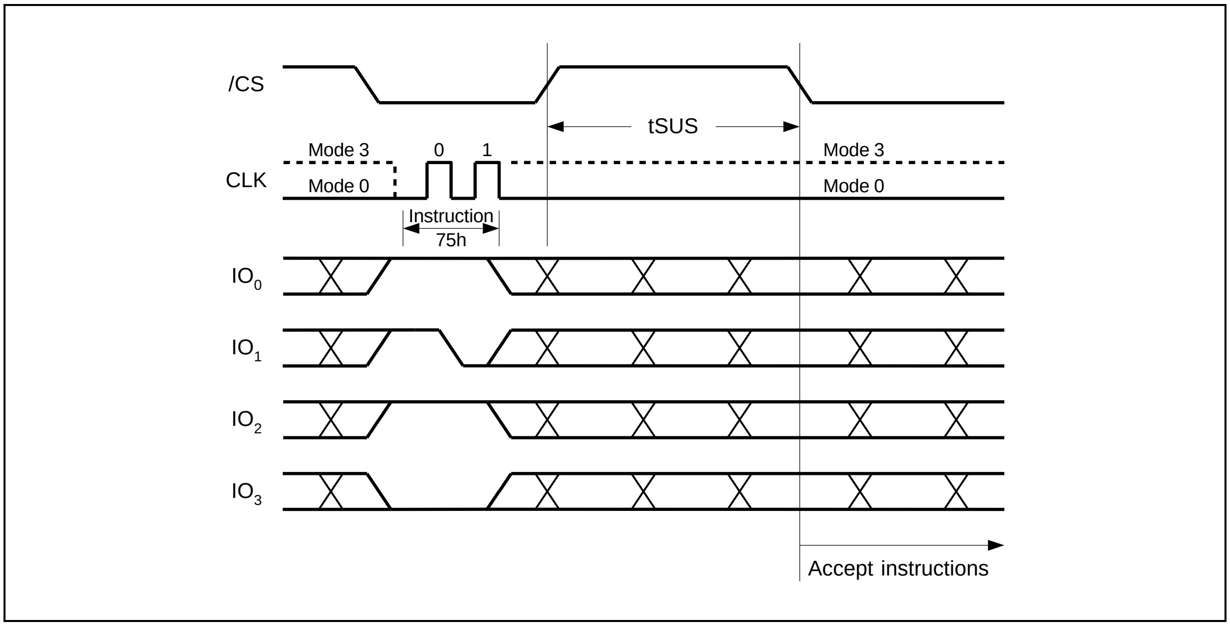


Figure 35b. Erase/Program Suspend Command (QPI Mode)

8.2.25 Erase / Program Resume (7Ah)

The Erase/Program Resume command "7Ah" must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume command "7Ah" will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume command "7Ah" will be ignored by the device. The Erase/Program Resume command sequence is shown in Figure 36a & 36b.

Resume command is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend command not to be issued within a minimum of time of "t_{SUS}" following a previous Resume command.

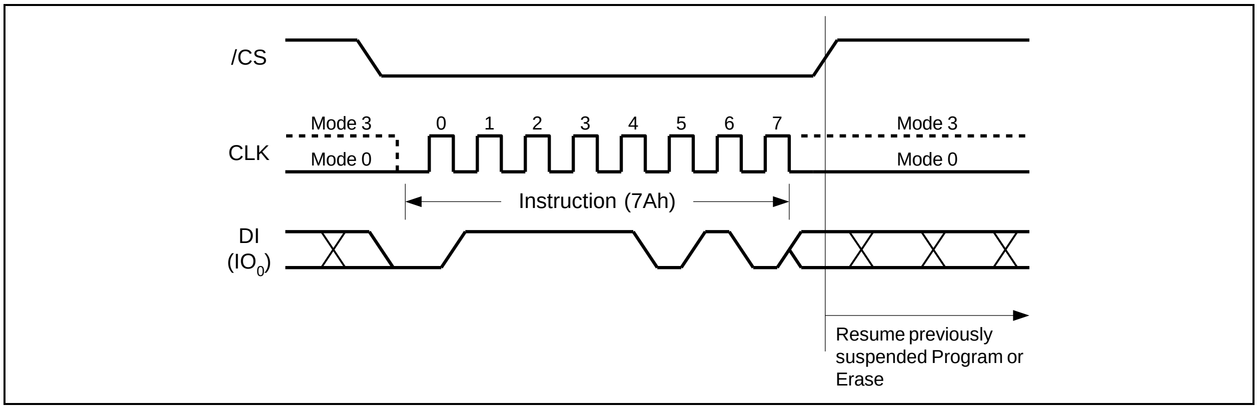


Figure 36a. Erase/Program Resume Command (SPI Mode)

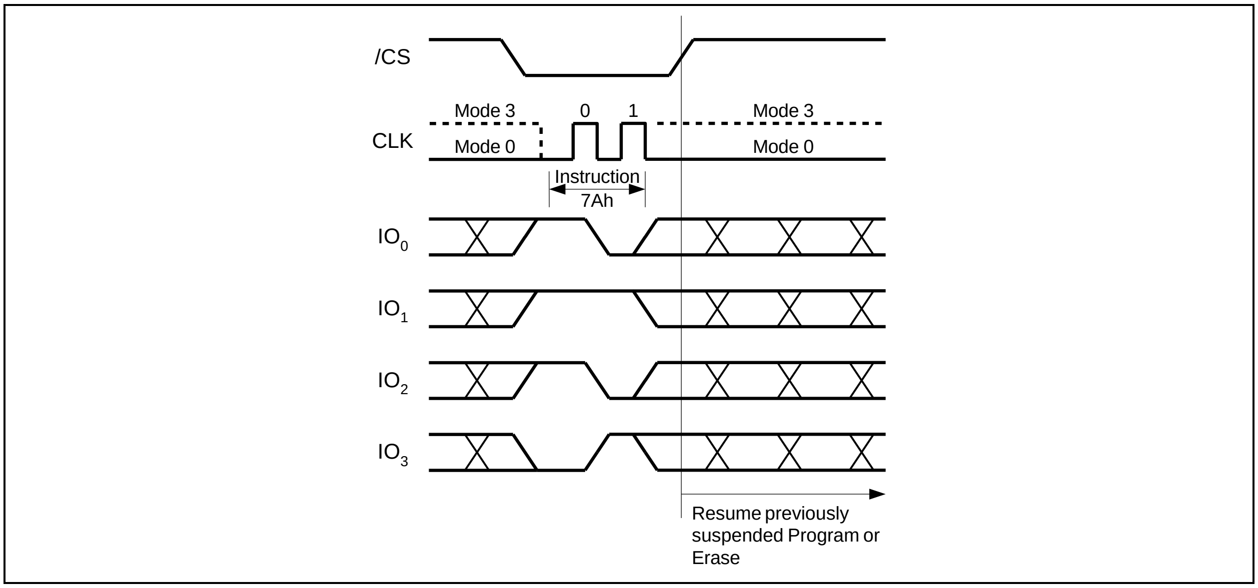


Figure 36b. Erase/Program Resume Command (QPI Mode)

8.2.26 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down command. The lower power consumption makes the Power-down command especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The command is initiated by driving the /CS pin low and shifting the command code "B9h" as shown in Figure 37a & 37b.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down command will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power-down / Device ID (ABh) command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

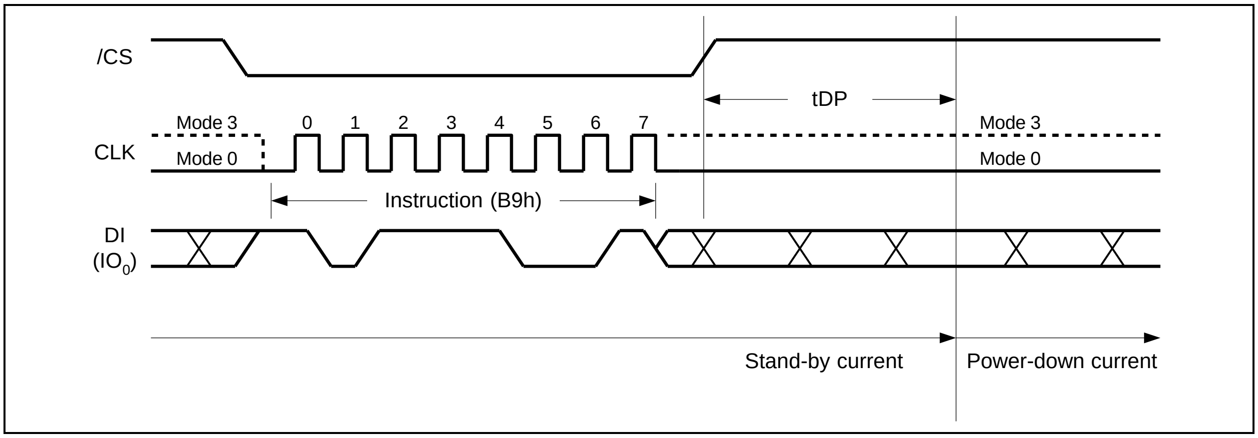


Figure 37a. Deep Power-down Command (SPI Mode)

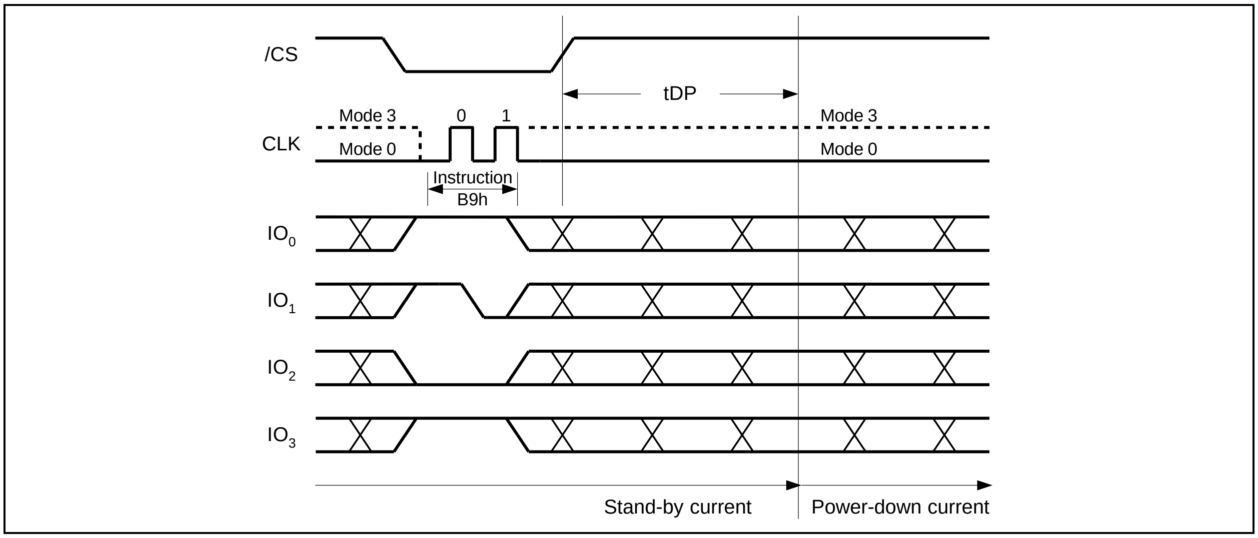


Figure 37b. Deep Power-down Command (QPI Mode)

8.2.27 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID command is a multi-purpose command. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the command is issued by driving the /CS pin low, shifting the command code "ABh" and driving /CS high as shown in Figure 38a & 38b. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other commands are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the command is initiated by driving the /CS pin low and shifting the command code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID value for the W25Q40/20/10RL is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 38c & 38d, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other commands will be accepted. If the Release from Power-down / Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the command is ignored and will not have any effects on the current cycle.

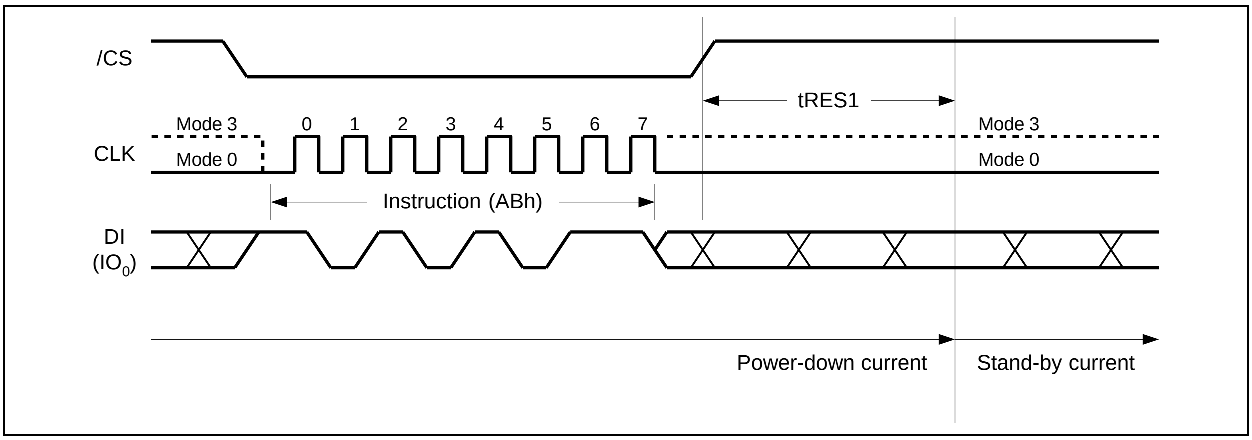


Figure 38a. Release Power-down Command (SPI Mode)

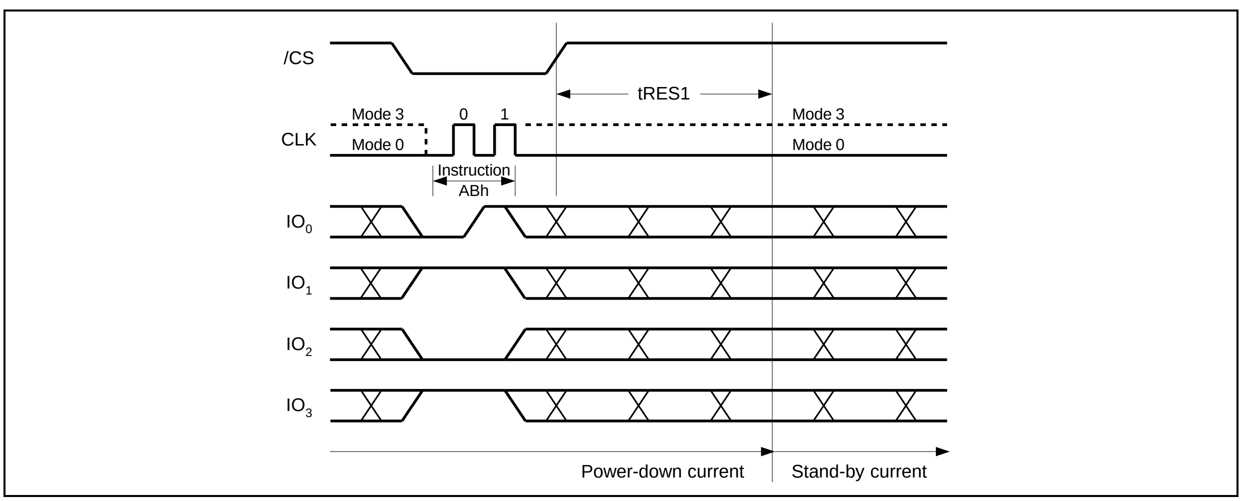


Figure 38b. Release Power-down Command (QPI Mode)

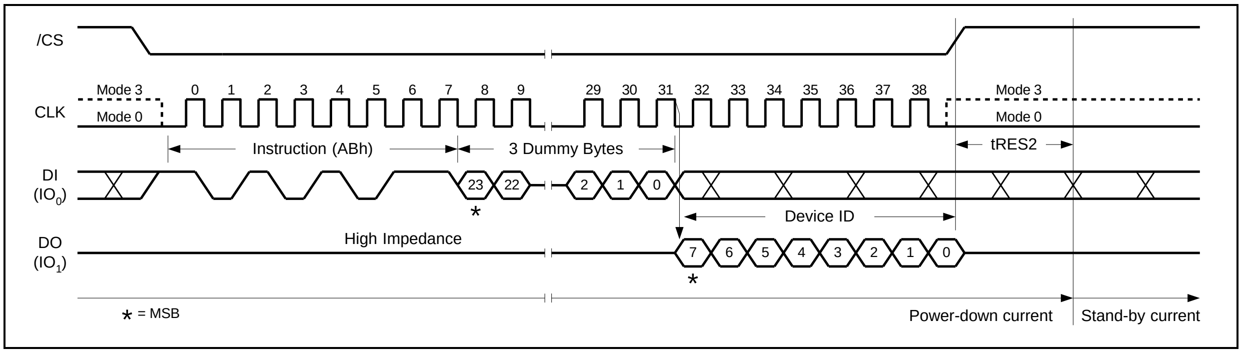


Figure 38c. Release Power-down / Device ID Command (SPI Mode)

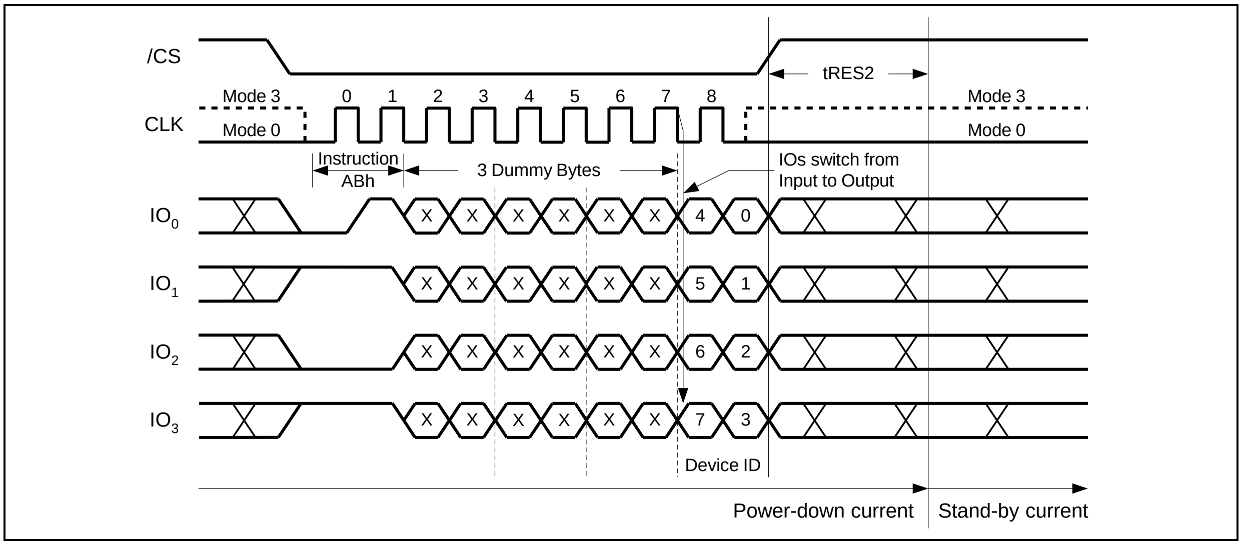


Figure 38d. Release Power-down / Device ID Command (QPI Mode)

8.2.28 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-down / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID command is very similar to the Release from Power-down / Device ID command. The command is initiated by driving the /CS pin low and shifting the command code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 39. The Device ID values for the W25Q40/20/10RL are listed in Manufacturer and Device Identification table. The command is completed by driving /CS high.

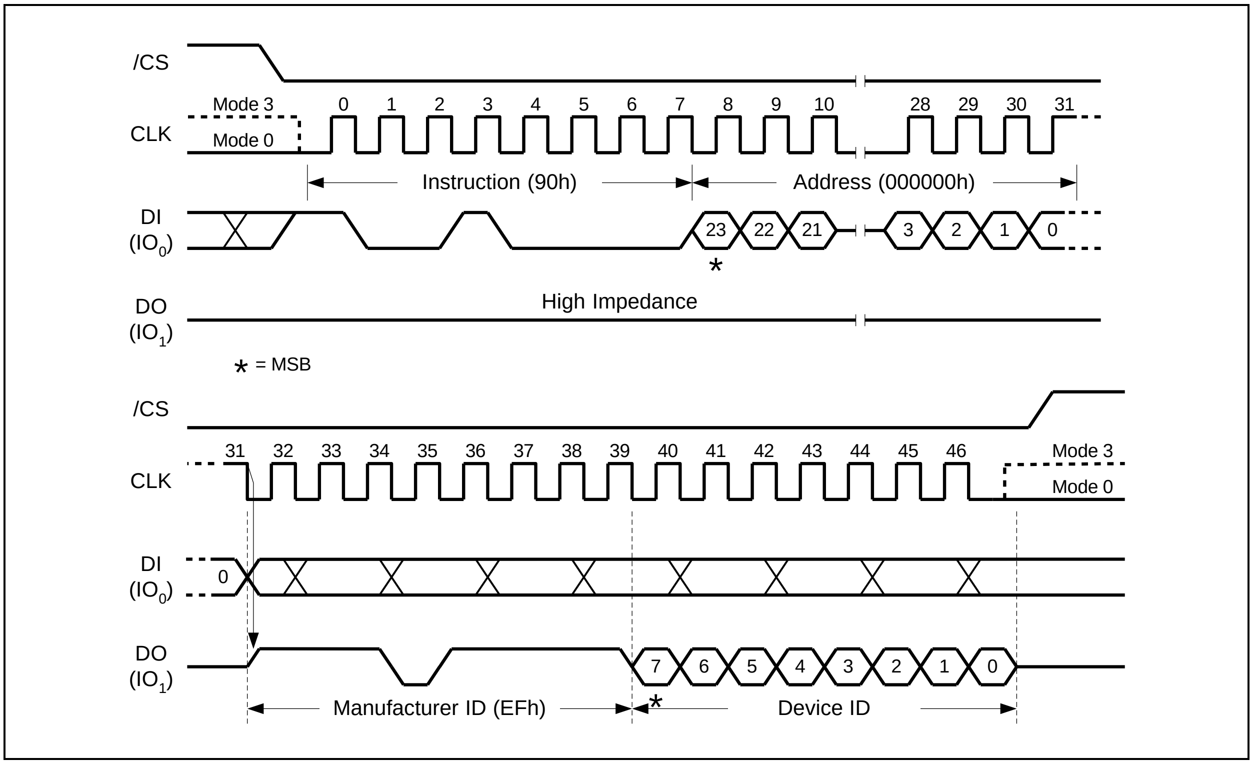


Figure 39. Read Manufacturer / Device ID Command (SPI Mode)

8.2.29 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O command is an alternative to the Read Manufacturer / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O Instruction is similar to the Fast Read Dual I/O Instruction. The Instruction is initiated by driving the /CS pin low and shifting the Instruction code "92h" followed by a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with the most significant bits (MSB) first as shown in Figure 40. The Device ID values for the W25Q40/20/10RL are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The Instruction is completed by driving /CS high.

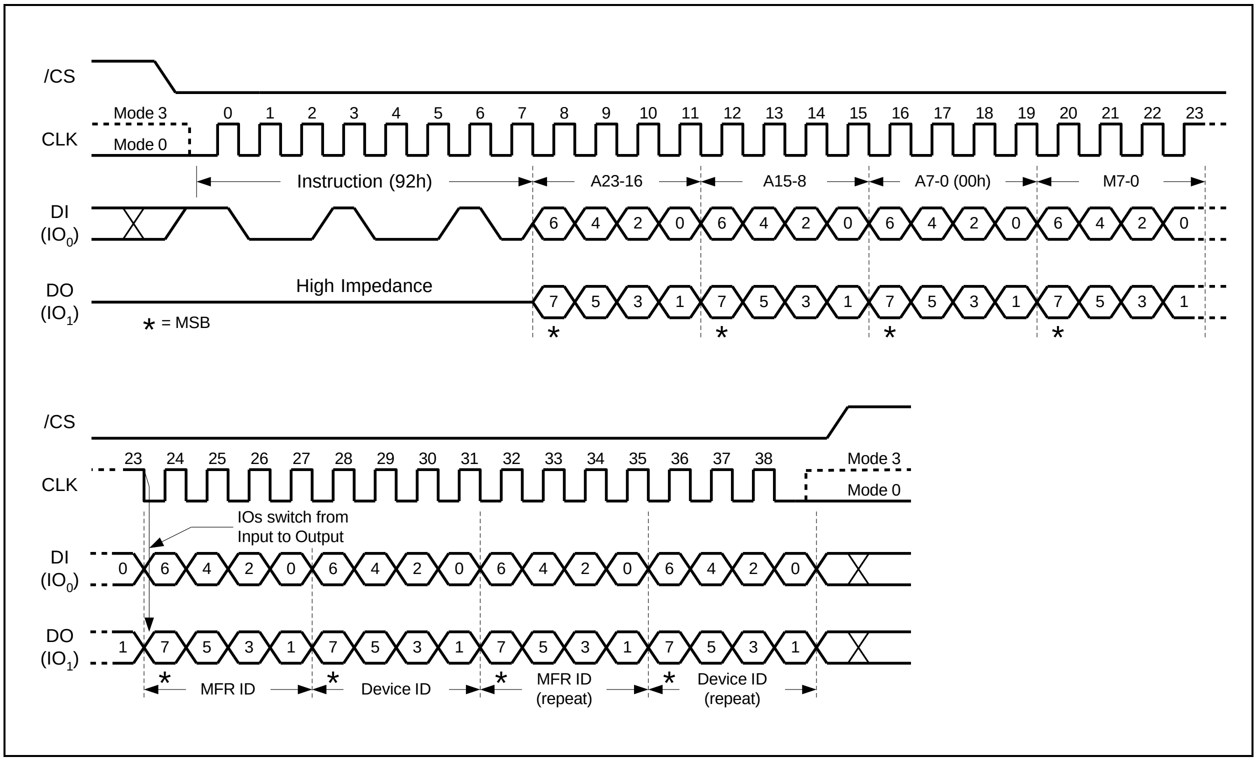


Figure 40. Read Manufacturer / Device ID Dual I/O Command (SPI Mode only)

Note:

The "Read Command Bypass Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O command.

8.2.30 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O command is an alternative to the Read Manufacturer / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O command is similar to the Fast Read Quad I/O command. The command is initiated by driving the /CS pin low and shifting the command code "94h" followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 41. The Device ID values for the W25Q40/20/10RL are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving /CS high.

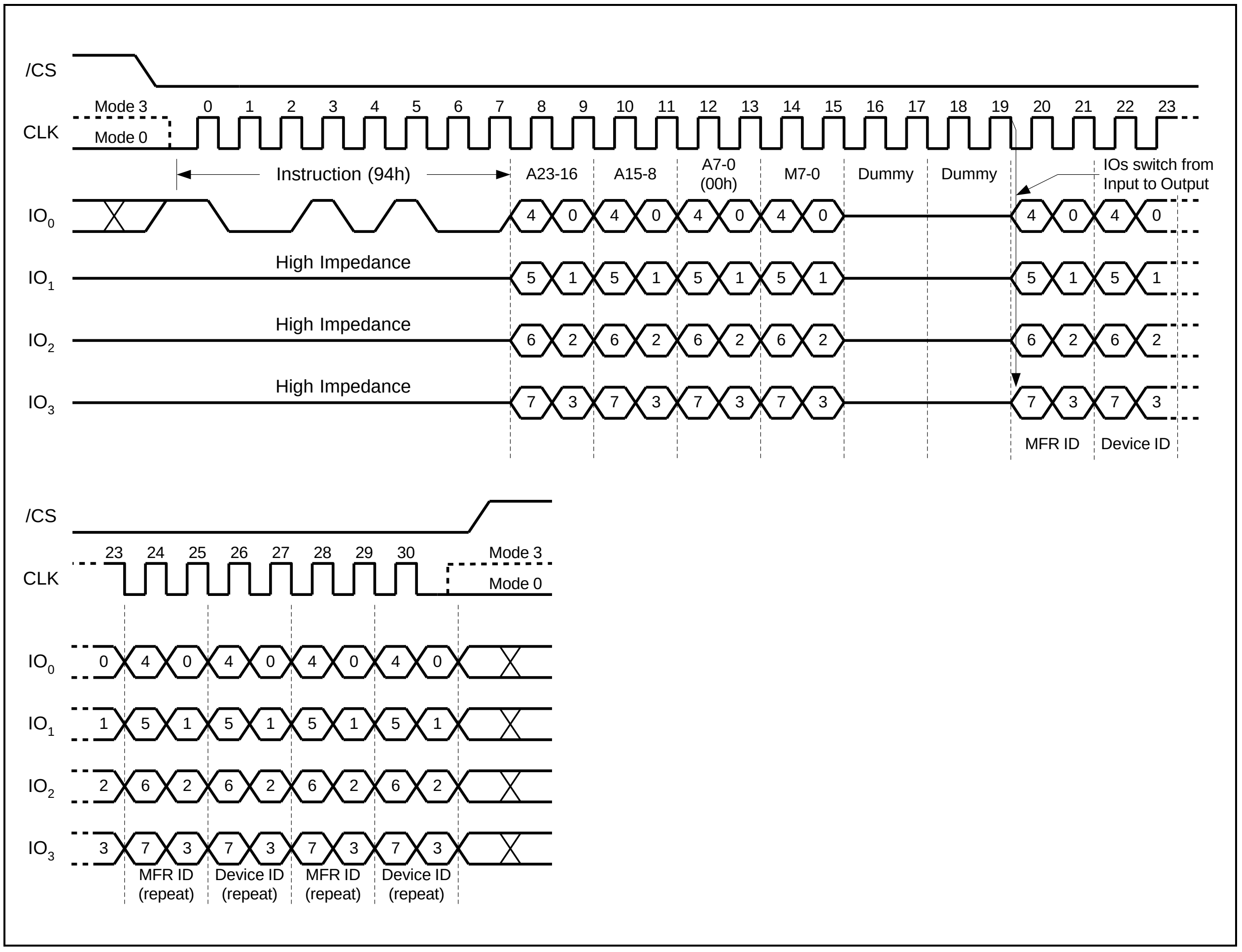


Figure 41. Read Manufacturer / Device ID Quad I/O Command (SPI Mode only)

Note:
The "Read Command Bypass Mode" bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O command.

8.2.31 Read Unique ID Number (4Bh)

The Read Unique ID Number command accesses a factory-set read-only 64-bit number that is unique to each W25Q40/20/10RL device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is initiated by driving the /CS pin low and shifting the command code “4Bh” followed by four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 42.

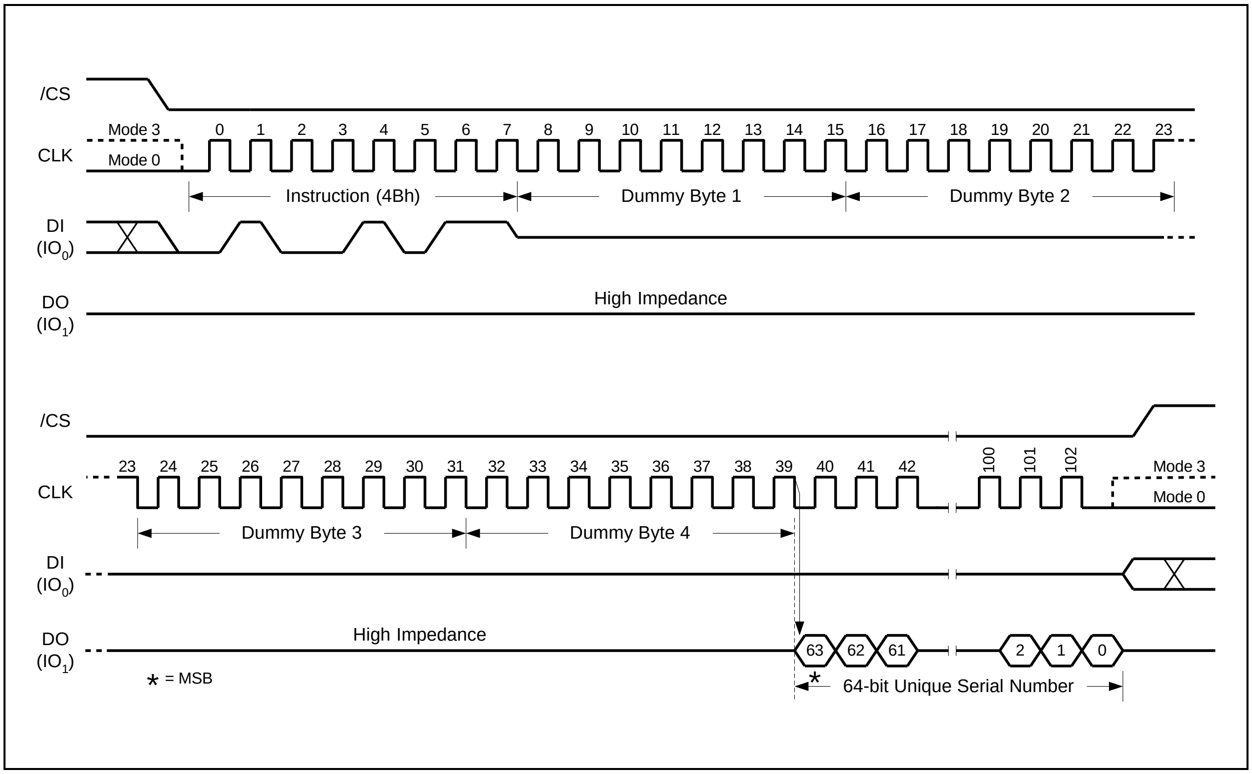


Figure 42. Read Unique ID Number Command (SPI Mode only)

8.2.32 Read JEDEC ID (9Fh)

For compatibility reasons, the W25Q40/20/10RL provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The command is initiated by driving the /CS pin low and shifting the command code "9Fh". The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 43a & 43b. For memory type and capacity values refer to Manufacturer and Device Identification table.

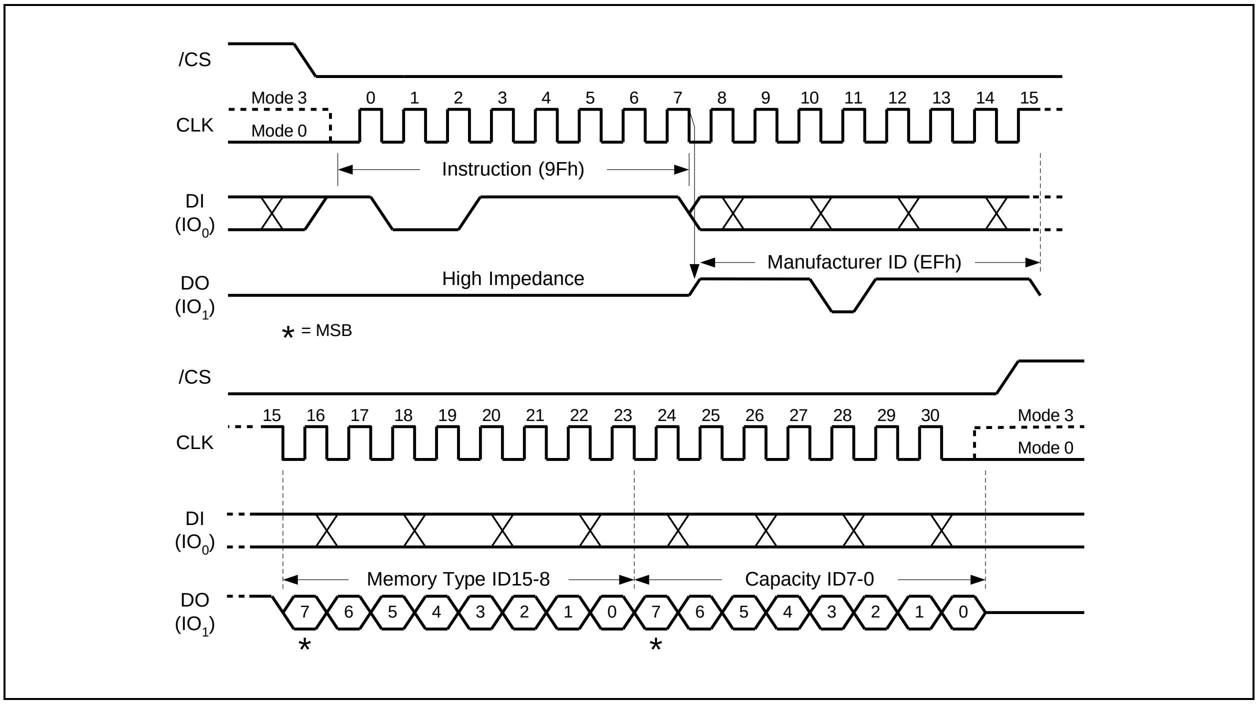


Figure 43a. Read JEDEC ID Command (SPI Mode)

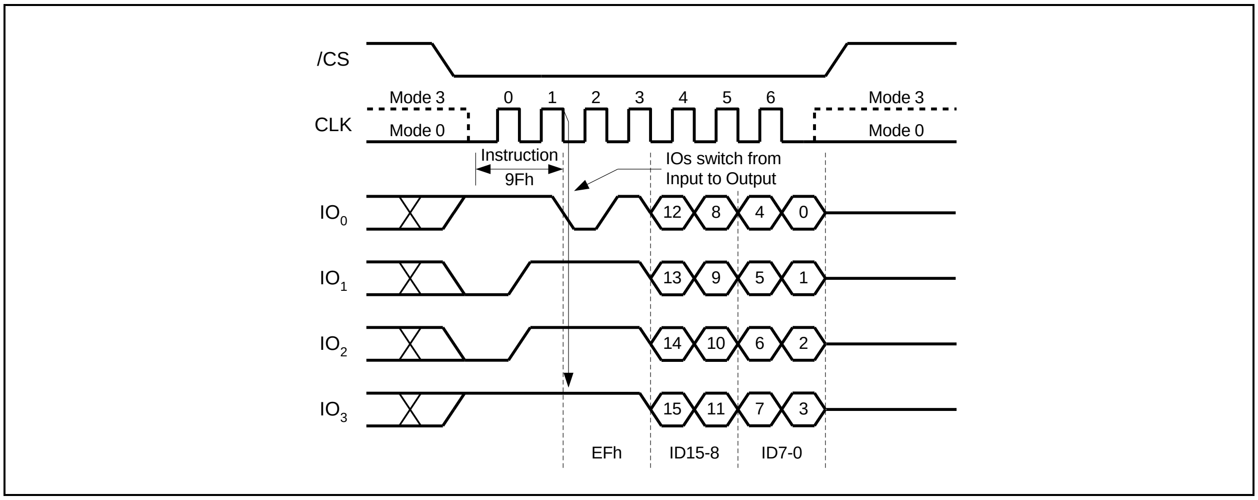


Figure 43b. Read JEDEC ID Command (QPI Mode)

8.2.34 Read SFDP Register (5Ah)

The W25Q40/20/10RL features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available commands and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register command is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216-serials that is published in 2011. The most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP command is initiated by driving the /CS pin low and shifting the command code “5Ah” followed by a 24-bit address (A23-A0)[(1)] into the DI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with the most significant bit (MSB) first as shown in Figure 44. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note 1: A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

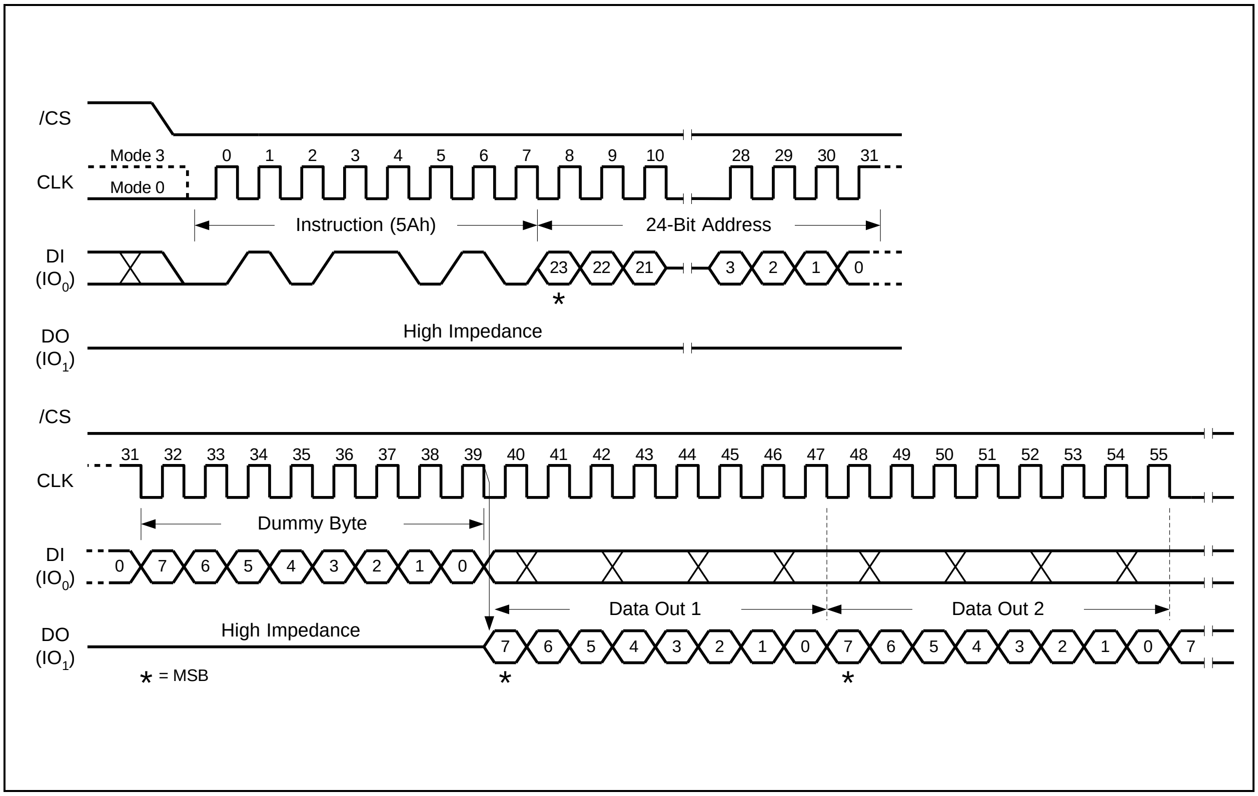


Figure 44. Read SFDP Register Command Sequence Diagram

8.2.35 Erase Security Registers (44h)

The W25Q40/20/10RL offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register command is similar to the Sector Erase command. A Write Enable command must be executed before the device will accept the Erase Security Register Command (Status Register bit WEL must equal 1). The command is initiated by driving the /CS pin low and shifting the command code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don’t Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don’t Care

The Erase Security Register Instruction sequence is shown in Figure 45. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register Instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other Instructions again. After the Erase Security Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and the Erase Security Register Instruction to that register will be ignored (Refer to section 7.1.8 for detail descriptions).

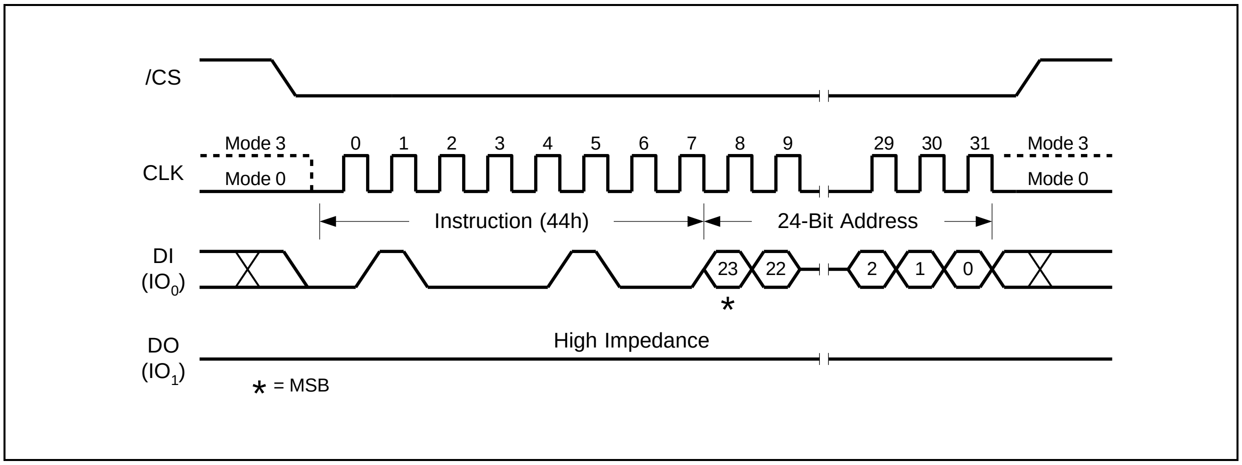


Figure 45. Erase Security Registers Command (SPI Mode only)

8.2.36 Program Security Registers (42h)

The Program Security Register command is similar to the Page Program command. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Program Security Register Command (Status Register bit WEL= 1). The command is initiated by driving the /CS pin low then shifting the command code "42h" followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the command while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register Instruction sequence is shown in Figure 46. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked and the Program Security Register Instruction to that register will be ignored (See 7.1.8, 8.2.25 for detail descriptions).

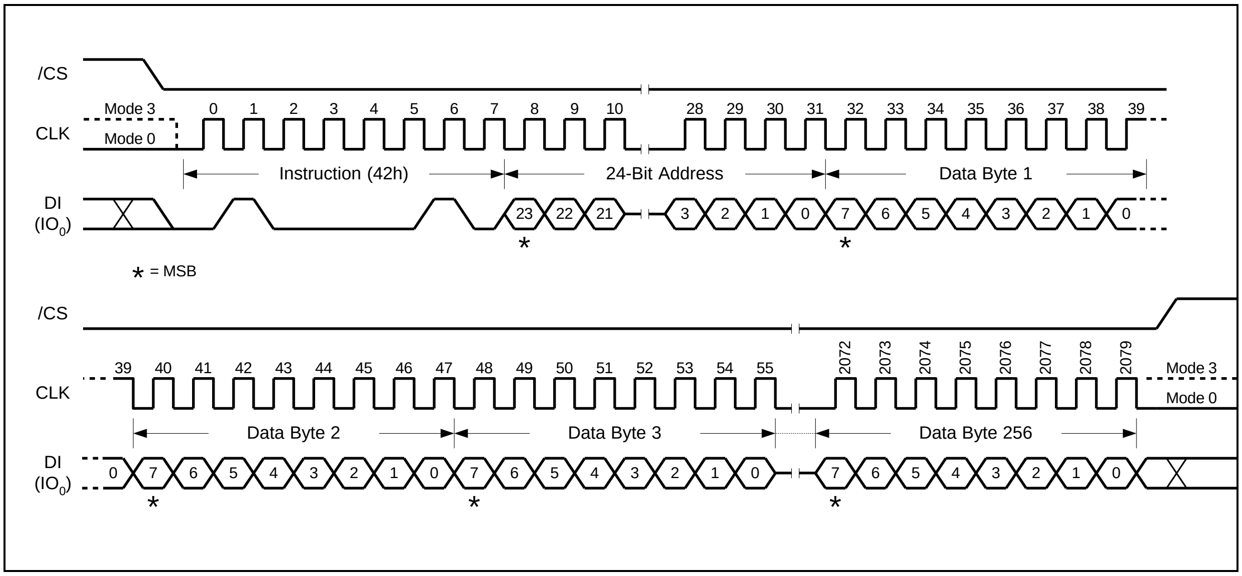


Figure 46. Program Security Registers Command (SPI Mode only)

8.2.37 Read Security Registers (48h)

The Read Security Register command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the four security registers. The command is initiated by driving the /CS pin low and then shifting the command code "48h" followed by a 24-bit address (A23-A0) and eight "dummy" clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The command is completed by driving /CS high. The Read Security Register command sequence is shown in Figure 47. If a Read Security Register command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle. The Read Security Register command allows clock rates from D.C. to a maximum of F_R (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

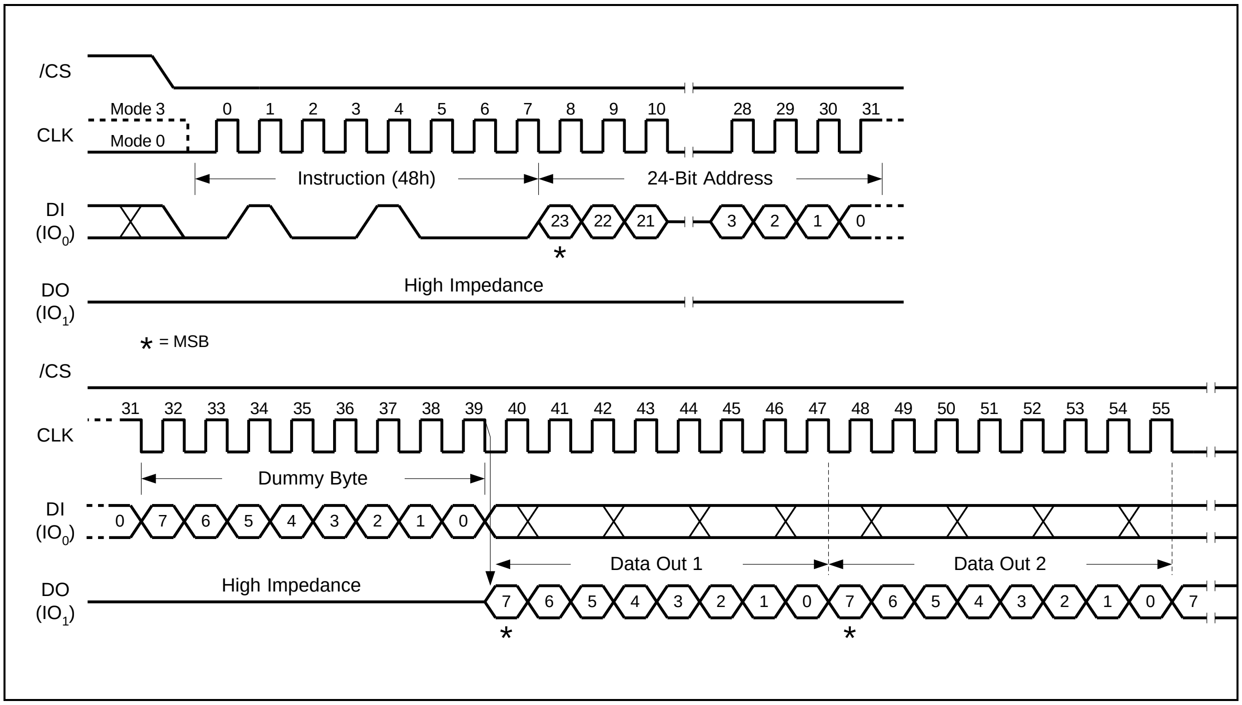


Figure 47. Read Security Registers Command (SPI Mode only)

8.2.38 Set Read Parameters (C0h)

In QPI/SPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “SPI/QPI Fast Read.”

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 6 for QPI/QPI. The number of dummy clocks is only programmable for Fast Read.

“Set Read Parameters (C0h)” instruction is used to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency. This is accomplished by setting the number of dummy clocks and wrap length configurations for set of selected instructions. Set Read Parameters (C0h) instruction writes to the Read Parameter Register (P[7:0]). P[6:4] bits is the dummy clocks configuration, while P[1:0] bits is the wrap length configuration for QPI mode only.

In SPI mode, SPI Set Read Parameters (C0h)" instruction writes to ‘Dummy Clocks’ P[6:4] bits only, while it will ignore ‘Wrap Length’ P[1:0] bits input as they are don’t care in SPI mode. Conversely, QPI Set Read Parameters instruction will write both to the P[6:4] and P[1:0] Read Parameter bits. The Set Read Parameters instruction sequence is shown in Figure 36.

The Set Read Parameters instruction (SPI or QPI) is used to configure the number of dummy cycles through the P[6:4] Read Parameter bits for the following SPI, QPI, DTR, and QPI DTR instructions:

- Standard SPI mode: Fast Read Quad I/O (EBh)
- QPI mode: Fast Read (0Bh), Fast Read Quad I/O (EBh), and Burst Read with Wrap (0Ch) instructions.
- SPI DTR mode: DTR Fast Read Quad I/O (EDh)
- QPI DTR mode: DTR Fast Read (0Dh) in QPI mode, DTR Fast Read Quad I/O (EDh) in QPI mode, and DTR Burst Read with Wrap (0Eh) in QPI mode instructions.

In QPI mode only, Set Read Parameters instruction to P[1:0] Read Parameter bits is used to configure the “Wrap Length” for the following QPI and QPI DTR read with wrap instructions:

- QPI mode: Burst Read with Wrap (0Ch) instruction.
- QPI DTR mode: DTR Burst Read with Wrap (0Eh) instruction.

QPI “Wrap Length” (P[1:0] bits) is the field setting for the number of bytes to burst read (8, 16, 32, or 64 bytes) before a wrap-around to the starting address. . The Wrap Length set by P[1;0] is only applicable in QPI mode and not in SPI mode. The “Fast Read Quad I/O (EBh)”, “Fast Read (0Bh)”, “DTR Fast Read Quad I/O (EDh)”**,** and **“**DTR Fast Read (0Dh)” instructions do not support wrap around feature in QPI mode.

The dummy clocks for various Fast Read instructions in Standard/Dual/Quad/DTR SPI mode are fixed, except for ”Fast Read Quad I/O (EBh)”, and “DTR Fast Read Quad I/O (EDh)” instructions. Please refer to the Instruction Tables 1-4 and 7-8 for details. “Wrap Length” for the SPI ”Fast Read Quad I/O (EBh)” and “DTR Fast Read Quad I/O (EDh)” instructions are set by W6-4 bit with the “Set Burst with Wrap (77h)” instruction.

The Wrap bits (Set Burst with Wrap ‘77h’) as well as Read Parameter bits P[7:0] setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode or vice versa. It is very important that the required dummy cycles and wrap length are set properly before executing the SPI (EBh), QPI (0Bh, EBh, 0Ch), DTR (EDh), and QPI DTR (0Dh, EDh, 0Eh) instructions.

The default Parameter Read “Dummy Clocks” and “Wrap Length“ settings for selected SPI, QPI, DTR, and QPI DTR read instructions after power up or reset are defined on the tables below. After power up or reset, Read Parameter bits are reset to 00h. Detailed Read Parameter bits configuration are also shown below.

SPI Dummy Clocks: EBh; ***QPI Dummy Clocks:*** 0Bh, EBh, 0Ch

SPI/ QPI P6 P5 P4	DUMMY CLOCKS	MAXIMUM(1) READ FREQ. 2.3V~3.6	MAXIMUM(1) READ FREQ. 2.7V~3.6
0 0 0	6(def)	104MHz	133MHz
0 0 1	6	104MHz	133MHz
0 1 0	6	104MHz	133MHz
0 1 1	8	104MHz	133MHz
1 0 0	10	104MHz	133MHz
1 0 1	12	104MHz	133MHz
1 1 0	14	104MHz	133MHz
1 1 1	16	104MHz	166MHz

QPI P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Note 1: 4-byte alignment Read address from “00.”

***SPI_DTR Dummy Clocks**: EDh.*
***QPI_DTR Dummy Clocks**:0Dh, EDh, 0Eh.*

DTR P6 P5 P4	DUMMY CLOCKS	MAXIMUM(1) READ FREQ. 2.3V~3.6	MAXIMUM(1) READ FREQ. 2.7V~3.6V
0 0 0	8(def)	66MHz	84MHz
0 0 1	8	66MHz	84MHz
0 1 0	8	66MHz	84MHz
0 1 1	8	66MHz	84MHz
1 0 0	8	66MHz	84MHz
1 0 1	8	66MHz	84MHz
1 1 0	8	66MHz	84MHz
1 1 1	16	66MHz	84MHz

Note 1: 4-byte alignment Read address from “00.”

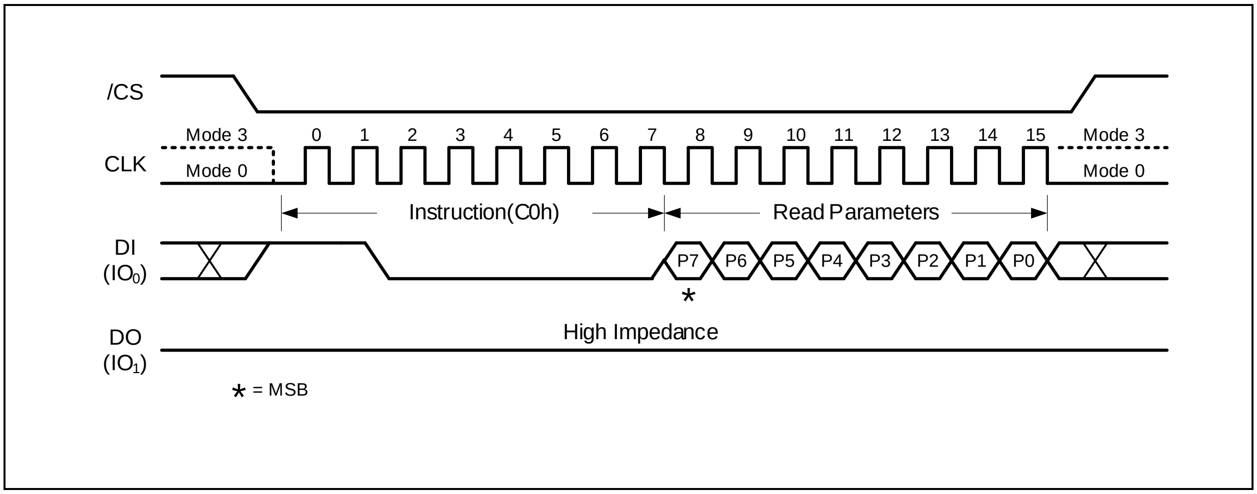


Figure 54. Set Read Parameters Instruction (SPI Mode)
"Set Read Parameters" instruction (C0h) can set the number of dummy clocks"

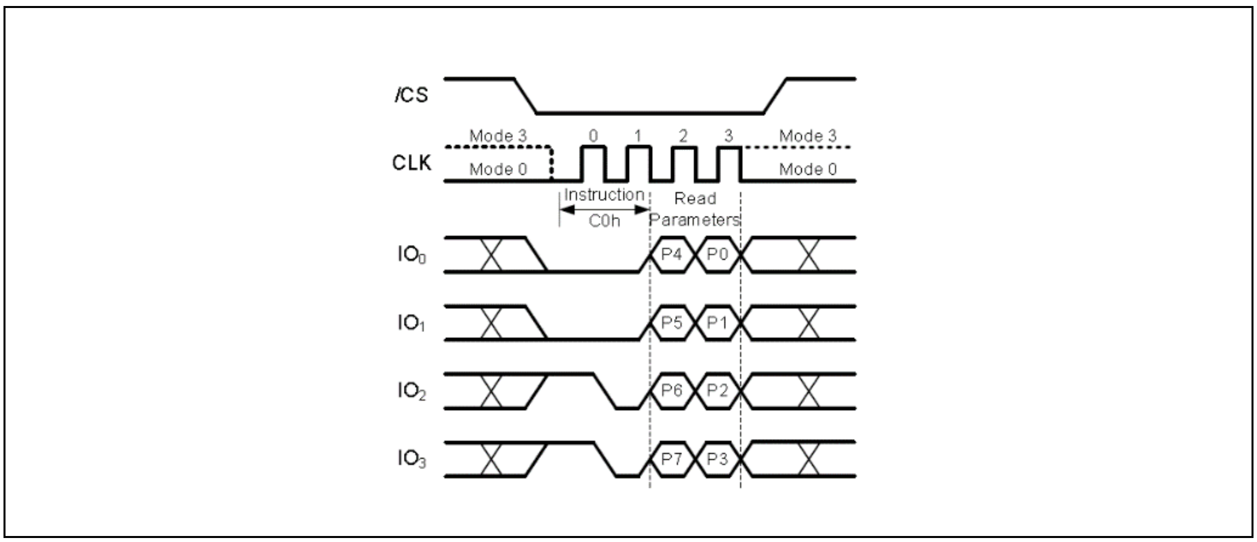


Figure 54. Set Read Parameters Instruction (QPI Mode)
"Set Read Parameters" instruction (C0h) can set the number of dummy clocks"

8.2.39 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The command is similar to the “Fast Read (0Bh)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” command. Refer to “Set Read Parameters (C0h)” for details.

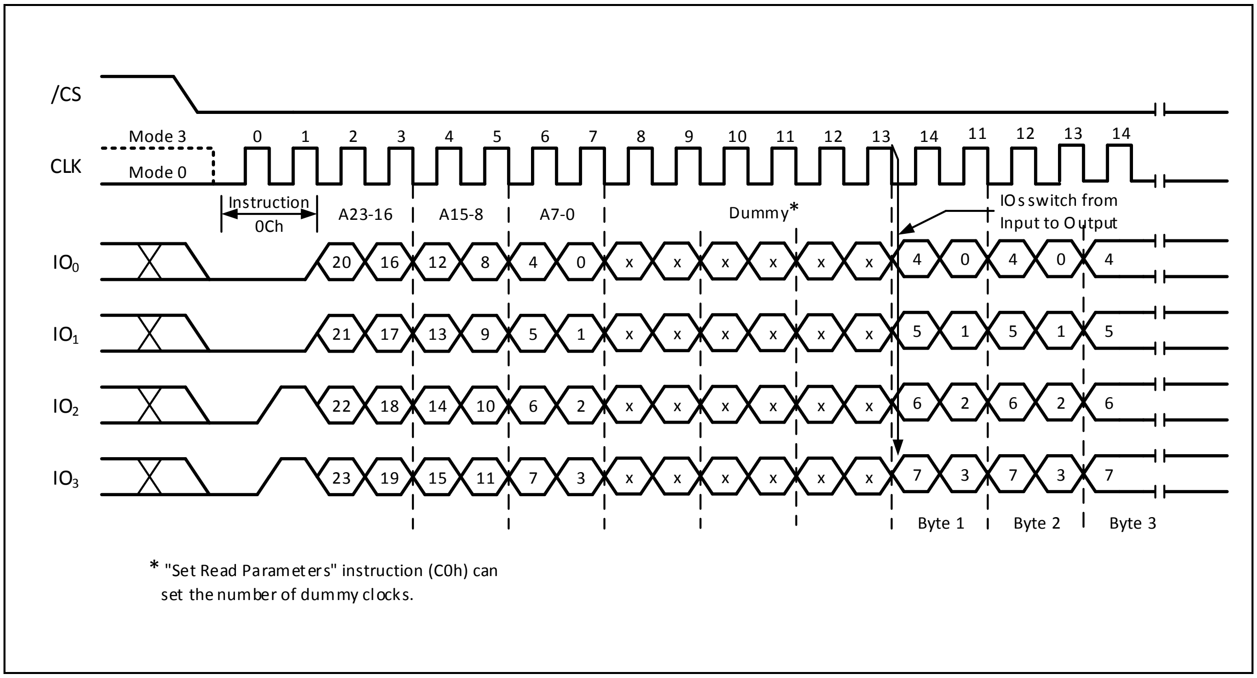


Figure 49. Burst Read with Wrap Command (QPI Mode only)

8.2.40 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by the “Set Read Parameters (C0h)” instruction. Refer to “Set Read Parameters (C0h)” for details.

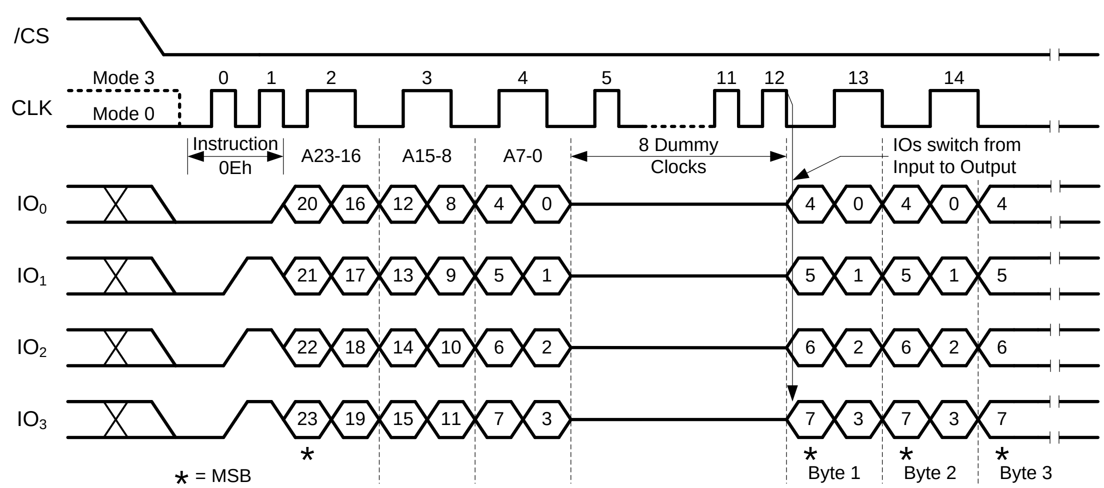


Figure 50. DTR Burst Read with Wrap Instruction (QPI Mode only)

8.2.41 Enter QPI Mode (38h)

The W25Q40/20/10RL support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” command is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Winbond serial flash memories. See Command Set Table 1-3 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” command must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” command will be ignored and the device will remain in SPI mode.

See Command Set Table 3 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

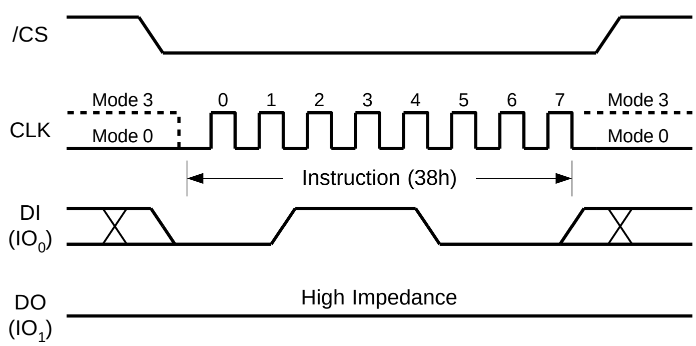


Figure 51. Enter QPI Command (SPI Mode only)

8.2.42 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” command must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

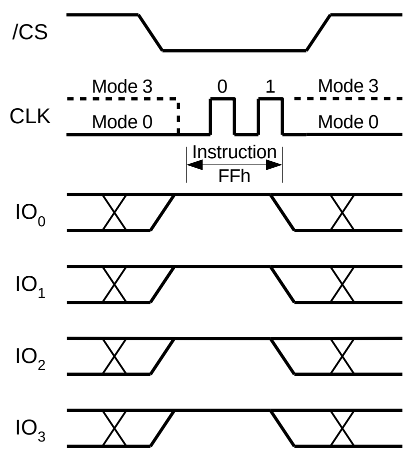


Figure 52. Exit QPI Command (QPI Mode only)

8.2.44 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25Q40/20/10RL provide a software Reset command instead of a dedicated RESET pin. Once the Reset command is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Read Command Bypass Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

"Enable Reset (66h)" and "Reset (99h)" commands can be issued in either SPI mode or QPI mode. To avoid accidental reset, both commands must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

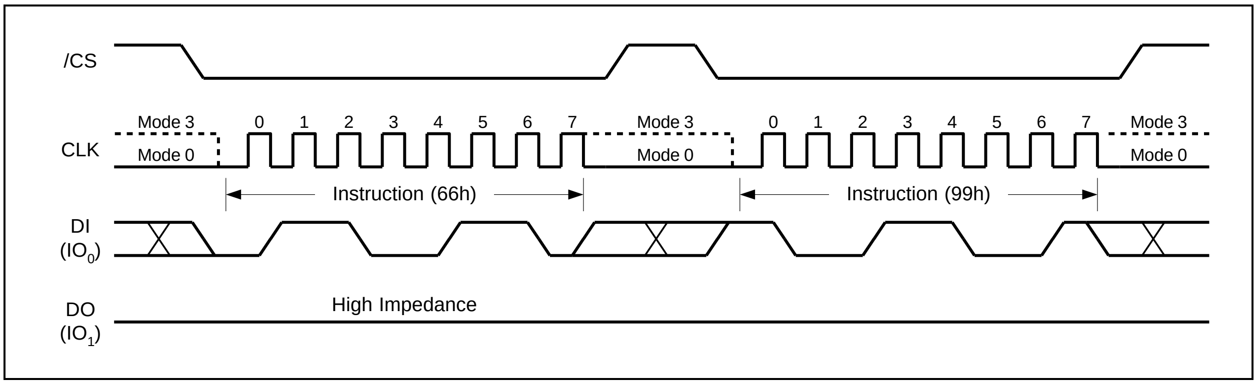


Figure 58a. Enable Reset and Reset Command Sequence (SPI Mode)

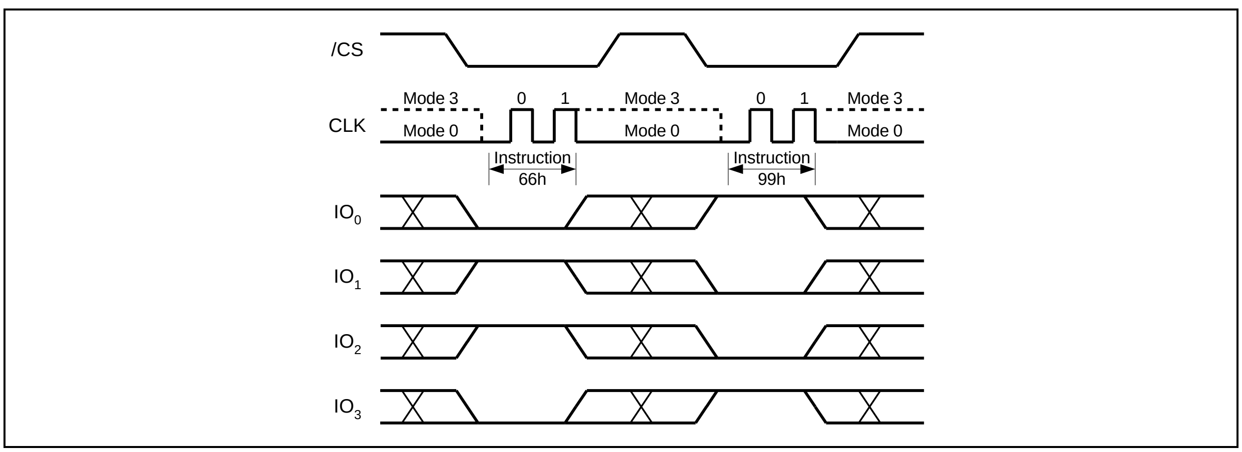


Figure 58b. Enable Reset and Reset Command Sequence (QPI Mode)

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings [1]

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 4.6	V
Voltage Applied to Any Pin	V_{IO}	Respect to VSS	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20nS Transient Respect to VSS	–2.0V to VCC+2.0V	V
Storage Temperature	T_{STG}		–65 to +150	°C
Lead Temperature	T_{LEAD}		See Note [2]	°C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model[3]	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage[1]	VCC	F_R = 133MHz, f_R = 84MHz	2.7	3.6	V
Supply Voltage[1]	VCC	F_R = 104MHz, f_R = 66MHz	2.3	2.7	V
Ambient Temperature, Operating	T_A	Industrial Plus	–40	+105	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

9.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	tVSL(1)	20		µs
Time Delay Before Write Command	tPUW(1)	5		ms
Write Inhibit Threshold Voltage	VWI(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

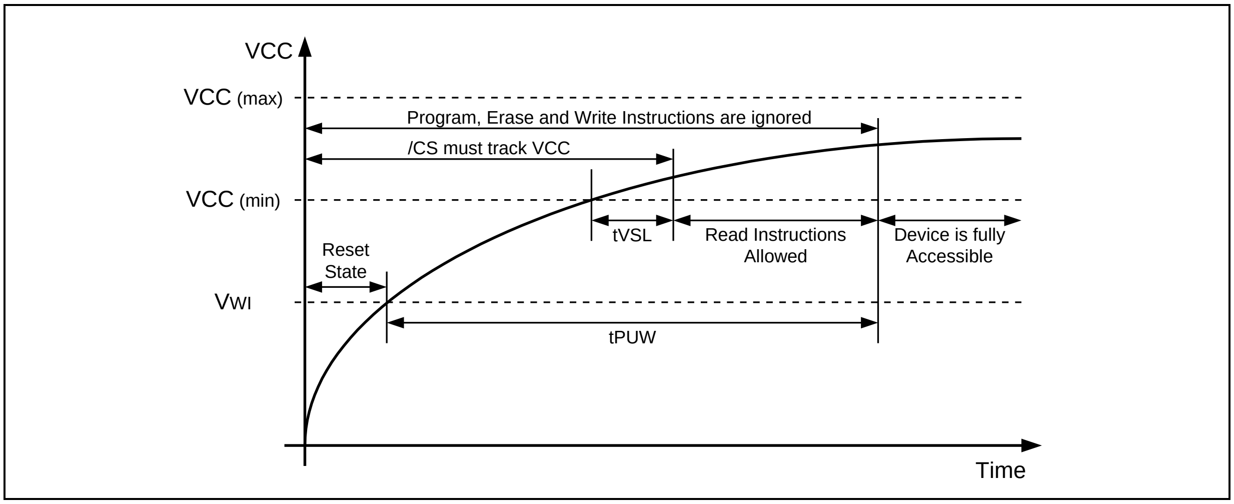


Figure 58a. Power-up Timing and Voltage Levels

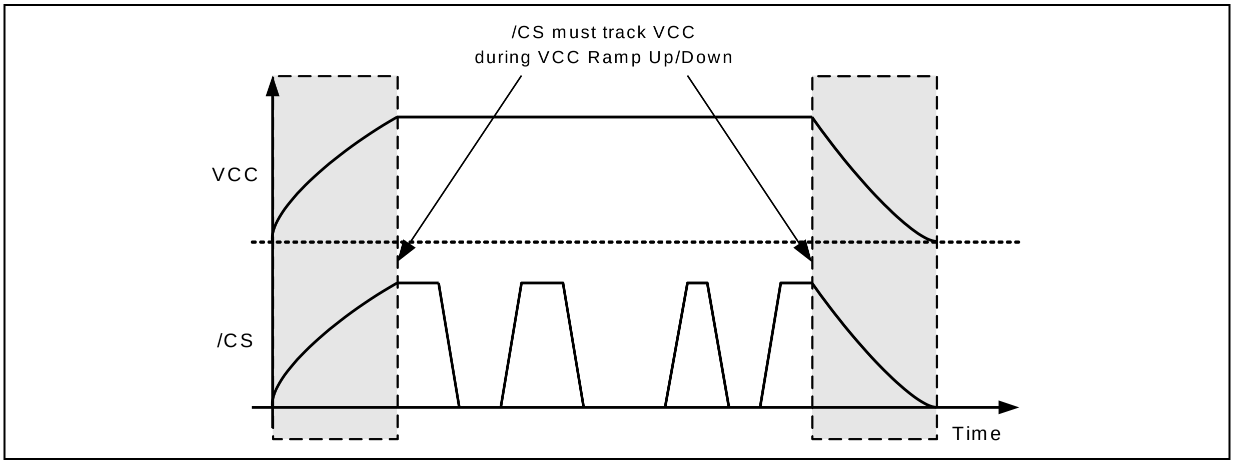


Figure 58b. Power-up, Power-Down Requirement

9.4 DC Electrical Characteristics(1)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	$I_{CC}1$	/CS = VCC, (≤85℃) VIN = GND or VCC		10	28(3)	µA
		/CS = VCC, (≤105℃) VIN = GND or VCC			35	µA
Power-down Current	$I_{CC}2$	/CS = VCC, VIN = GND or VCC		0.1	5	µA
Read Data / Dual /Quad 50MHz(2) Current	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		6	12	mA
Read Data / Dual /Quad 84MHz(2) Current	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		7	15	mA
Read Data / Dual /Quad 104MHz(2) Current	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		9	18	mA
Read Data / Dual /Quad 133MHz(2) Current	$I_{CC}3$	C = 0.1 VCC / 0.9 VCC DO = Open		11	20	mA
Write Status Register Current	$I_{CC}4$	/CS = VCC		8	15	mA
Page Program Current	$I_{CC}5$	/CS = VCC		8	15	mA
Sector/Block Erase Current	$I_{CC}6$	/CS = VCC		8	15	mA
Chip Erase Current	$I_{CC}7$	/CS = VCC		8	15	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.
2. Checker Board Pattern.
3. Value guaranteed by design and/or characterization, not 100% tested in production.

9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

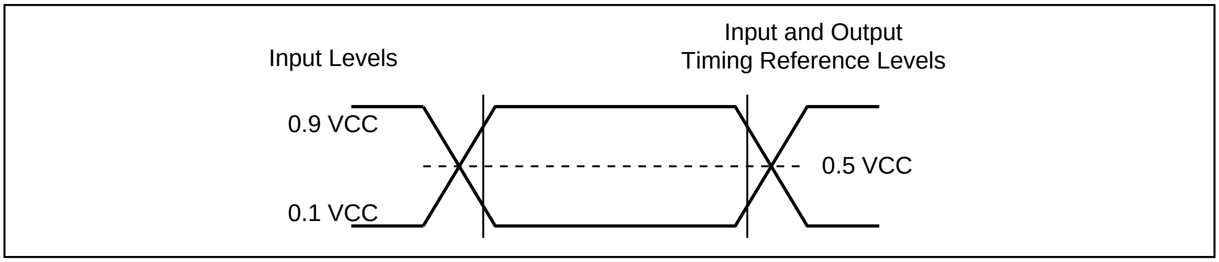


Figure 59. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics[6]

DESCRIPTION	SYMBOL	ALT	SPEC MIN	SPEC TYP	SPEC MAX	UNIT
Clock frequency for SPI & QPI commands except for Read Data (03h) & DTR (2.7~3.6V)	F_R	f_{C1}	D.C.		133[6]	MHz
Clock frequency for SPI & QPI commands except for Read Data (03h) & DTR (2.3~2.7V)	F_R	f_{C1}	D.C.		104[6]	MHz
Clock frequency DTR instructions (2.7~3.6V)	F_R	f_{C1}	D.C.		84[6]	MHz
Clock frequency DTR instructions (2.3~2.7V)	F_R	f_{C1}	D.C.		66[6]	MHz
Clock frequency for Read Data command (03h) (2.7~3.6V)	f_R		D.C.		84[6]	MHz
Clock frequency for Read Data command (03h) (2.3~2.7V)	f_R		D.C.		66[6]	MHz
Clock High, Low Time for all commands except for Read Data (03h)	t_{CLH}, t_{CLL}[1]		45%P_C			ns
Clock High, Low Time for Read Data (03h) command	t_{CRLH}, t_{CRLL}[1]		45%P_C			ns
Clock Rise Time peak to peak	t_{CLCH}[2]		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}[2]		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time — 2.7-3.6V VCC	t_{CHDX}	t_{DH}	2.5			ns
Data In Hold Time — 2.3-2.7V VCC			3			
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Read) — 2.7-3.6V VCC	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Read) — 2.3-2.7V VCC			12.5			
/CS Deselect Time (for Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}[2]	t_{DIS}			7	ns
Clock Low to Output Valid — 2.7-3.6V VCC	t_{CLQV}	t_V			4.5	ns
Clock Low to Output Valid — 2.3-2.7V VCC					6	

Continued – next page AC Electrical Characteristics (cont'd)

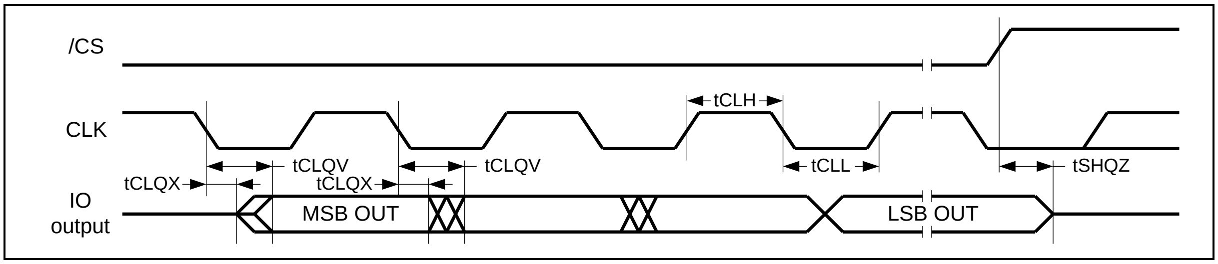
AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Output Hold Time	t_{CLQX}	t_{HO}	1			ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with ID Read	t_{RES2}(2)				1.8	µs
/CS High to next Command after Suspend	t_{SUS}(2)				20	µs
/CS High to next Command after Reset	t_{RST}(2)				30	µs
/RESET pin Low period to reset the device(5)	t_{RESET}(2)		1(4)			µs
Write Status Register Time	t_W			1.5	15	ms
Page Program Time	t_{PP}			0.25	2	ms
Sector Erase Time (4KB)	t_{SE}			30	240	ms
Block Erase Time (32KB)	t_{BE1}			80	800	ms
Block Erase Time (64KB)	t_{BE2}			120	1,200	ms
Chip Erase Time -W25Q40RL	t_{CE}			0.8	5	s
Chip Erase Time -W25Q20RL	t_{CE}			0.5	2.5	s
Chip Erase Time -W25Q10RL	t_{CE}			0.25	1.25	s

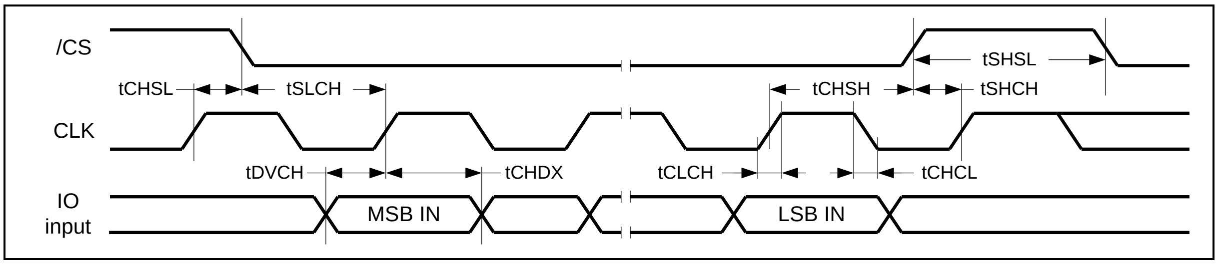
Notes:

1. Clock high or Clock low must be more than or equal to 45%Pc. Pc=1/$f_{C(MAX)}$
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register command when SRP=1.
4. It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. T_A = 25° C, VCC = 3.0V, 50-Ohm driver strength.
6. 4-bytes address alignment for Read, start address from [A1,A0]=(0,0).

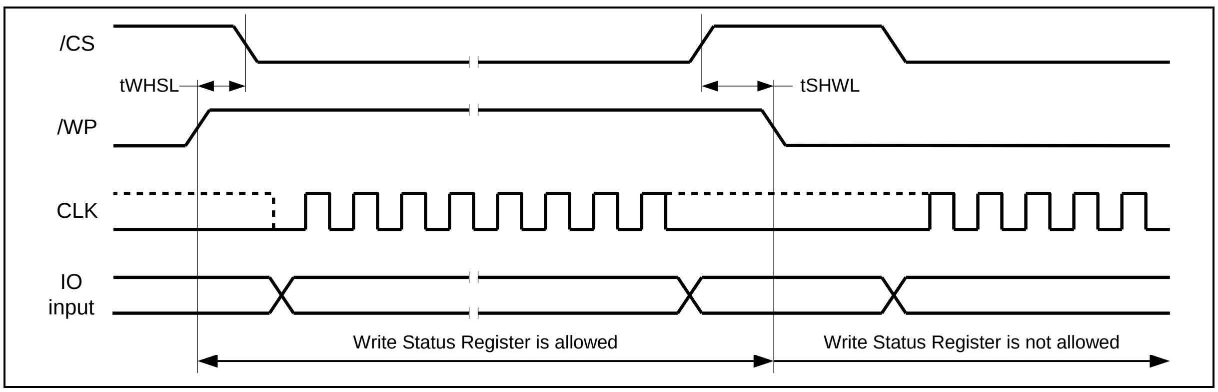
9.7 Serial Output Timing



9.8 Serial Input Timing

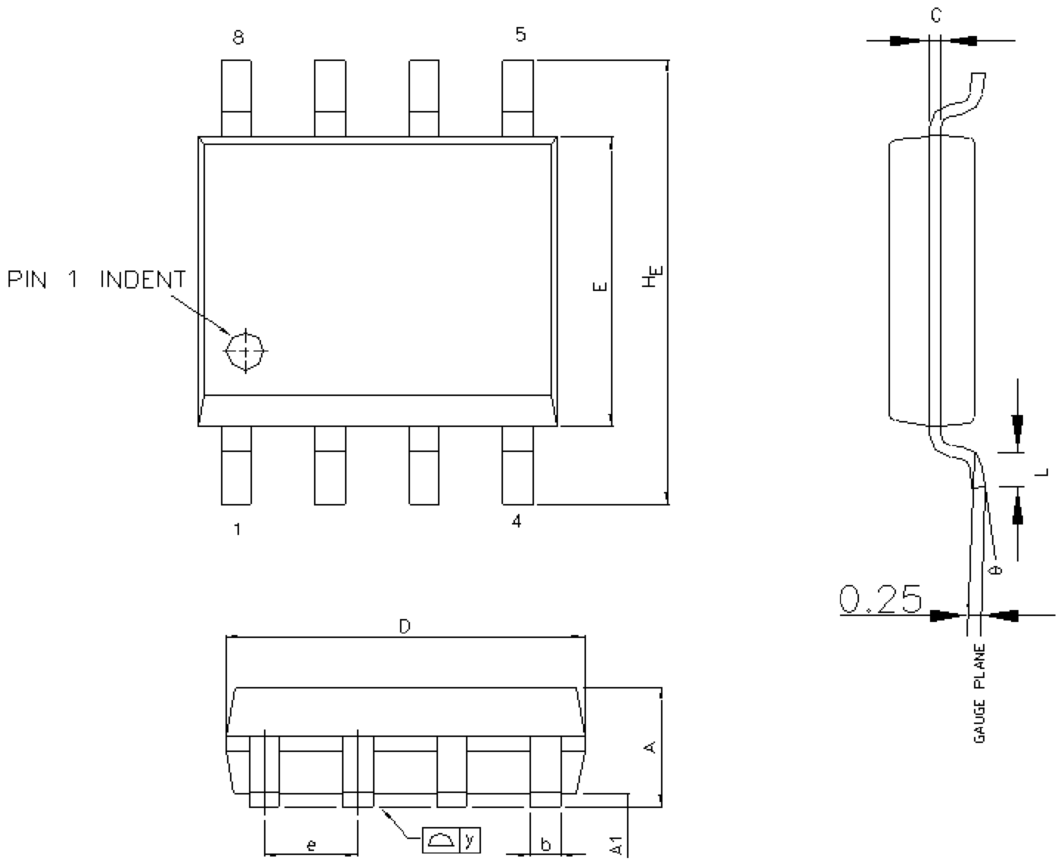


9.9 WP Timing



10. PACKAGE SPECIFICATIONS

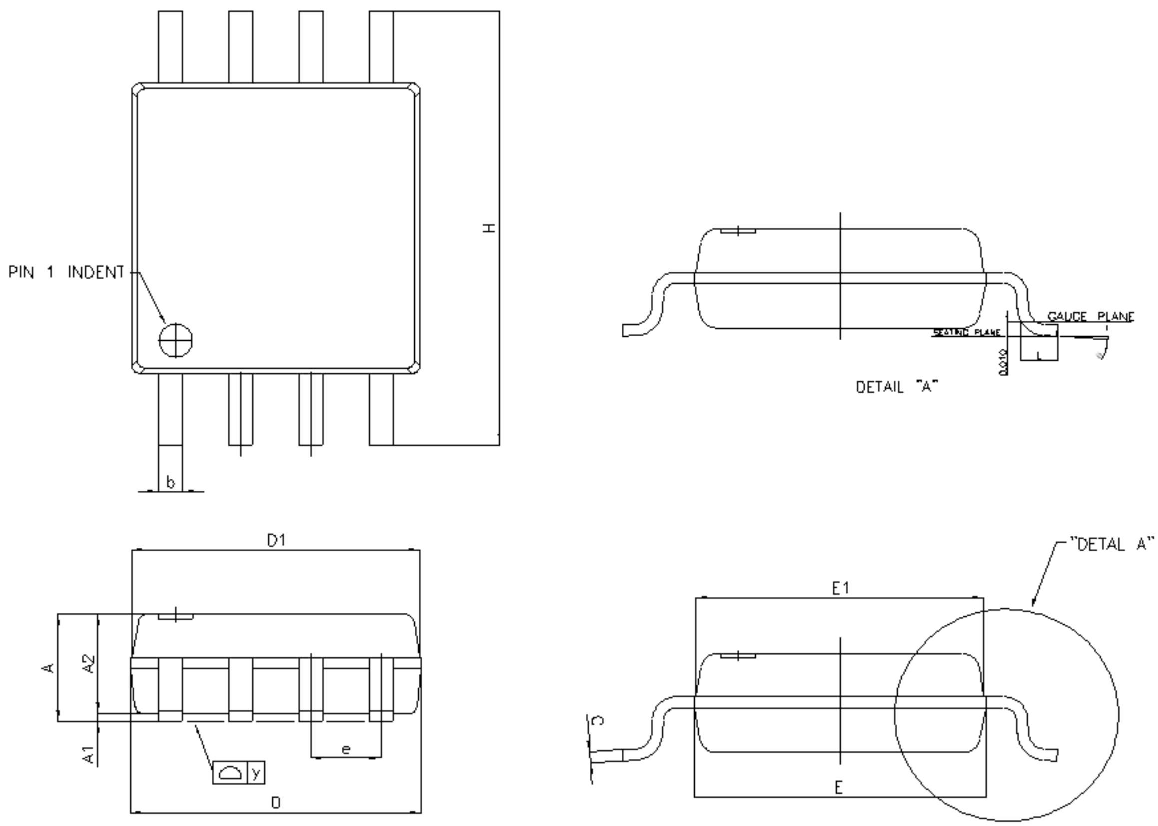
10.1 8-Pin SOIC 150-mil (Package Code SN)



SYMBOL	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.60	1.75	0.053	0.062	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.0078	0.0098
D	4.80	4.85	5.00	0.188	0.190	0.197
E	3.80	3.90	4.00	0.150	0.153	0.157
H_E	5.80	6.00	6.20	0.288	0.236	0.244
e	1.27BSC			0.050BSC		
L	0.40	0.71	1.27	0.016	0.027	0.050
y	---	---	0.10	---	---	0.004
θ°	0°	---	10°	0°	---	10°

Note: Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

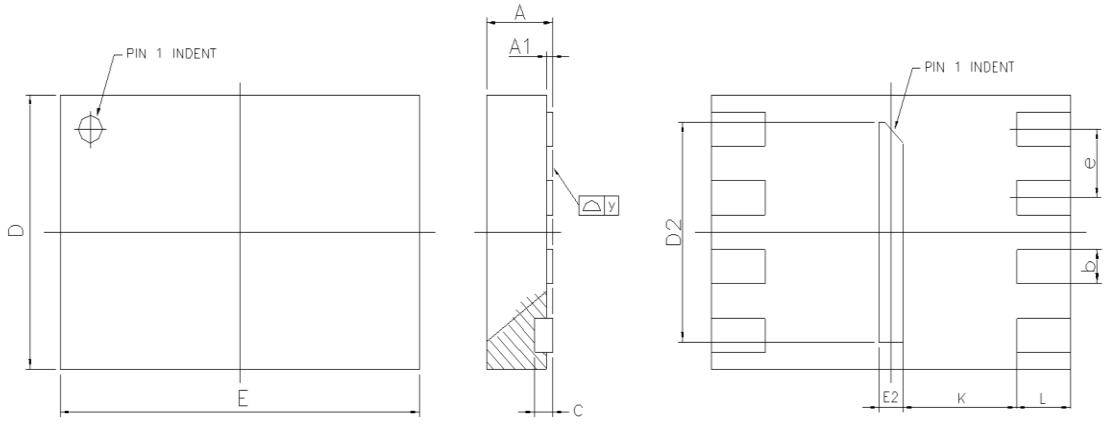
10.2 8-Pin SOIC 208-mil (Package Code SS)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
D1	5.13	5.23	5.33	0.202	0.206	0.210
E	5.18	5.28	5.38	0.204	0.208	0.212
E1	5.13	5.23	5.33	0.202	0.206	0.210
e	1.27 BSC			0.050 BSC		
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

Note: Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)

10.3 8-Pad XSON 2x3x0.4-mm (Package Code XH)



Symbol	Millimeters		
	Min	Nom	Max
A	0.30	0.35	0.40
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C	---	0.127 Ref.	---
D	1.90	2.00	2.10
D2	1.55	1.60	1.65
E	2.90	3.00	3.10
E2	0.15	0.20	0.25
e	---	0.50	---
K	0.95 Ref.		
L	0.40	0.45	0.50
y	0.00	---	0.075

Note:

The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.

11. ORDERING INFORMATION

W[(1)] 25Q xxR L xx[(2)] J x

Company Prefix

W = Winbond

Product Family

25Q = SpiFlash Serial Flash Memory with 4KB sectors, Dual/Quad I/O

Product Number / Density

40R = 4M-bit   20R = 2M-bit

10R = 1M-bit

Supply Voltage

L = 2.3V to 3.6V

Package Type

SN = 8-pin SOIC 150-mil   SS = 8-pin SOIC 208-mil

XH = 8-pad XSON 2x3-mm

Temperature Range

J = Industrial Plus (-40°C to +105°C)

Special Options[(3,4)]

M[(3,4,5)] = With QE = 0 (Non-fixed) in Status register-2.

Notes:

1. The "W" prefix is not included on the part marking.
2. Only the 2nd letter is used for the part marking; WSON package type ZP are not used for the part marking.
3. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
4. For shipments with OTP feature enabled, please contact Winbond.
5. All devices are in compliance of RoHs, Halogen free, TSCA, and REACH.

11.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25Q40/20/10RL SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150-mil	4M-bit	W25Q40RLSNJM	25Q40RLNJM
SS SOIC-8 208-mil	4M-bit	W25Q40RLSSJM	25Q40RLSJM
XH(1,2) XSON-8 2x3x0.4(max.)mm³	4M-bit	W25Q40RLXHJM	* X3ywH JMxxxx(3)

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150-mil	2M-bit	W25Q20RLSNJM	25Q20RLNJM
XH(1,2) XSON-8 2x3x0.4(max.)mm³	2M-bit	W25Q20RLXHJM	* X2ywH JMxxxx(3)

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150-mil	1M-bit	W25Q10RLSNJM	25Q10RLNJM
XH(1,2) XSON-8 2x3x0.4(max.)mm³	1M-bit	W25Q10RLXHJM	* X1ywH JMxxxx(3)

Note:

1. These package types are special order, please contact Winbond for more information.
2. XSON. has special top side marking due to size limitation
3. “yw” is date code
   “xxxx” is lot ID

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	05/03/2024		New create
B	05/06/2024	88-89	Added Note for SOP-150/208mil
C	09/09/2024	92	Updated top side marking of W25Q40RLXHJM
D	02/18/2025	83 85	Added ICC1 @85°C value Updated tCHDX at 2.3~2.7V

Trademarks

Important Notice

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